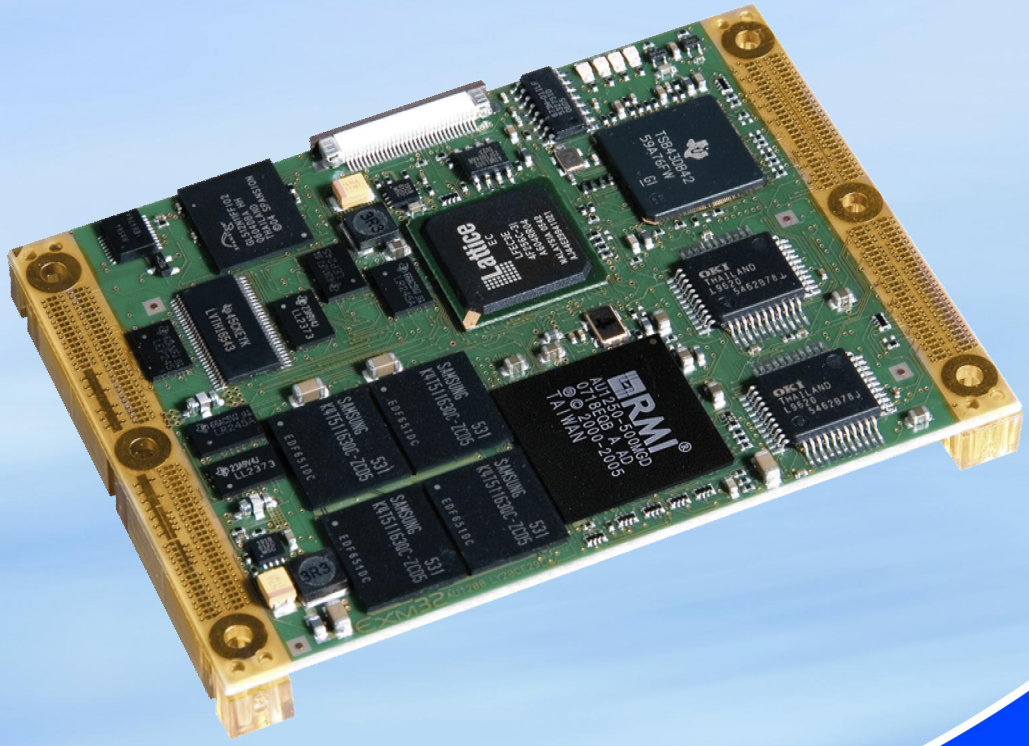

MSC
EXM32-Au1250
CPU-Module

User's Manual

Revision 1.0
Hardware Revision V5.0

MICROCOMPUTERS · SYSTEMS · COMPONENTS · VERTRIEBS GMBH

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Preface

Copyright Notice

Important Information

This documentation is intended for qualified audience only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

Disclaimer

Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided "as is" and is subject to change without notice.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Trademarks

All used product names, logos or trademarks are property of their respective owners.

Certification

MSC Vertriebs GmbH is certified according to DIN EN ISO 9001:2000 standards.

Life-Cycle-Management

MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product-change-notification and end-of-life management process assures early information of our customers.

Product Support

MSC engineers and technicians are committed to provide support to our customers whenever needed.
Before contacting Technical Support of MSC Vertriebs GmbH, please consult the respective pages on our web site at www.msc-ge.com/support-boards for the latest documentation, drivers and software downloads.
If the information provided there does not solve your problem, please contact our Technical Support:

Email: support.boards@msc-ge.com
Phone: +49 8165 906-200

Contents

Document change history

Date	*Version*	*Document change description*
2005-09-14	01	EXM32 AU1200 CPU Module - Initial Version
2008-03-12	08	Update to EXM32 AU1250 CPU Module V30
2008-09-08	09	Register Definition Update
2008-09-17	1.0	released

1 General Information

1.1 Introduction

The EXM32 Au1250 CPU Module is designed to operate with an EXM32 compatible motherboard to form a complete system. The motherboard will provide power supply and legacy interface connectors, as required by the specific application. With the possibility to add expansion modules, an EXM32 system can be easily adopted to very specific applications, such as gigabit transmission interfaces, wireless communication, etc… An example EXM32 system is shown in figure 1:

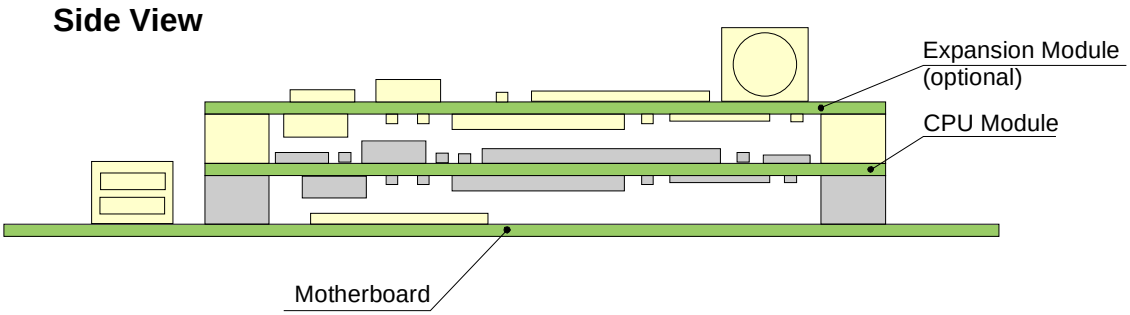


Figure 1: EXM32 System

Special notice is given to meet the enhanced environment requirements in automotive and industrial applications: the EXM32 system is designed to

EXM32 is a new form factor to develop compact industrial control systems. It is small enough for most applications, yet provides enough space to implement complete systems with very few modules. Special notice is given to meet the enhanced environment requirements in industrial applications: EXM32 CPU modules can operate in the extended industrial temperature range and meet DIN EN 60068 (environmental conditions for electrical and electronic equipment for road vehicles).

The revolutionary EXM32 connector technology uses very reliable elastomeric contact elements in a robust shell. This is no plug and socket system, only one EXM32 connector element is used for every connector location. This allows also an easy preparation of system extensions without cost penalty.

The inter-board connection between Module and Motherboard or between two modules is established by compressing the contact elements in between two module boards that have matching contact pads. The connection has 'zero insertion force', is compressed and secured by screws and therefore withstands shock and vibration.

1.2 Functional Blocks

The EXM32 Au1250 CPU Module includes the following functional blocks:

CPU

AMD Alchemy Au1250 (MIPS) CPU 500 MHz

Memory (on-board)

up to 256 MByte DDR-RAM (32 bit bus-width)
up to 128 Mbyte linear Flash (16 bit bus-width)
optional NAND Flash up to 256 Mbyte (8 bit bus-width)

Peripherals

Au1250 integrated LCD STN/TFT controller with a maximum resolution 2048x2048 pixel.

PCMCIA/CF Interface (dual slot supported)

Camera Interface

Ethernet 10/100T Controller
USB 2.0 high Speed OTG Host/Function controller (2-port)
CAN (2x)
Asynchr. Serial Interface (2x)
I2C(3x)
SPI
AC97/I²S Sound Interface
RTC

Bus

The 16-Bit (optional 32-Bit) CPU bus for SRAM- or VLIO-type peripherals available on module connector (buffered, 5V tolerant). EXM32 allows to stack multiple CPU modules that share the motherboard's or extension module's resources .

Connectors

Two EXM32 Connectors carries all interfaces, the system CPU bus and the power supply.

A Debug connector allows the connection of an JTAG based debug tool.

1.2.1 Block Diagram

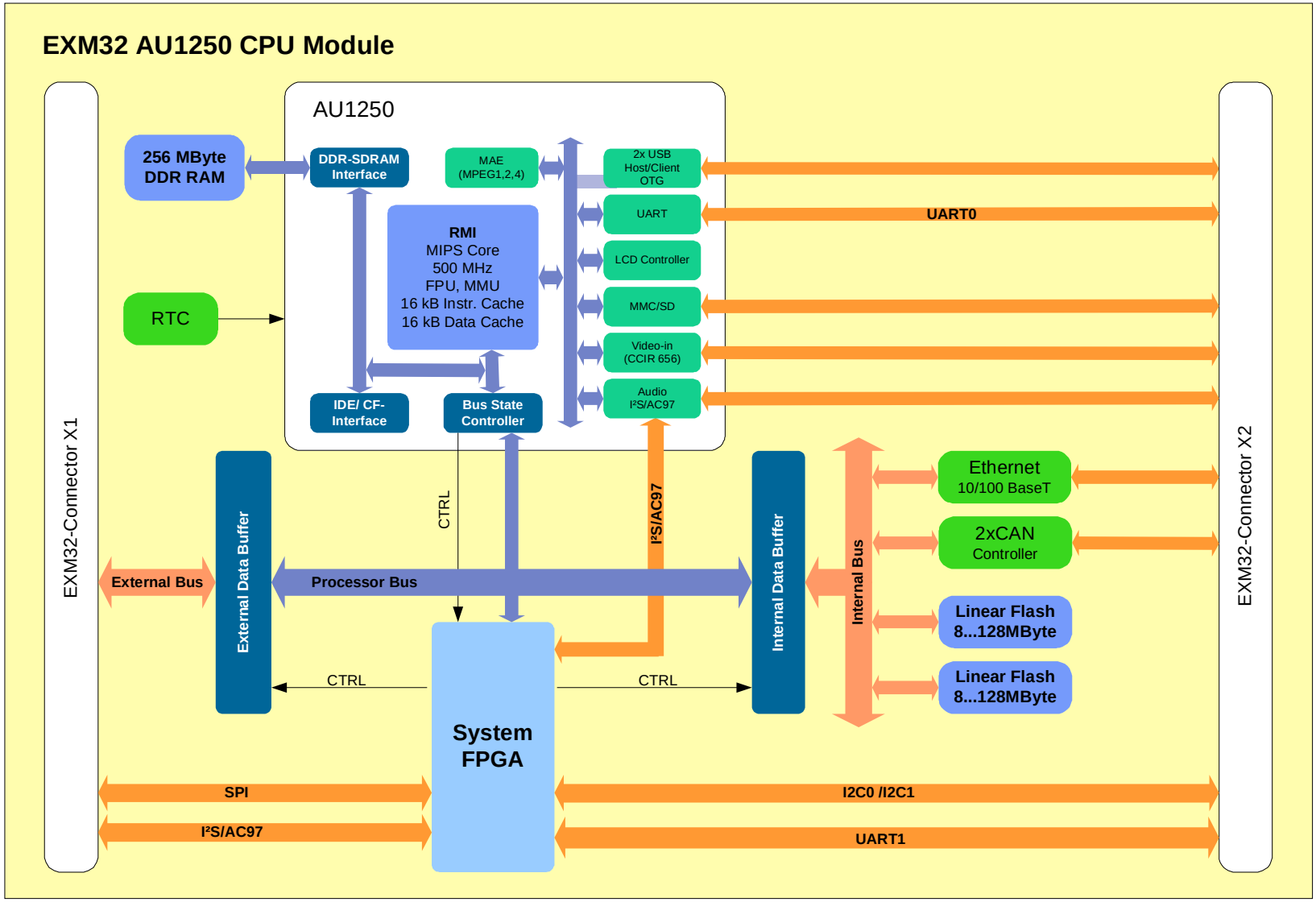


Figure 2: EXM32-Au1250 block diagram

2 Overview

2.1 Connectors

EXM32 Connectors

Two EXM32 208 pin connectors. These connectors support EXM32 compatible modules.

Debug Connector

Allows the connection of an JTAG based Debugger Tool.

Board type

Compact CPU module size 90 x 65 mm, stackable with other EXM32 modules.

2.2 Specification

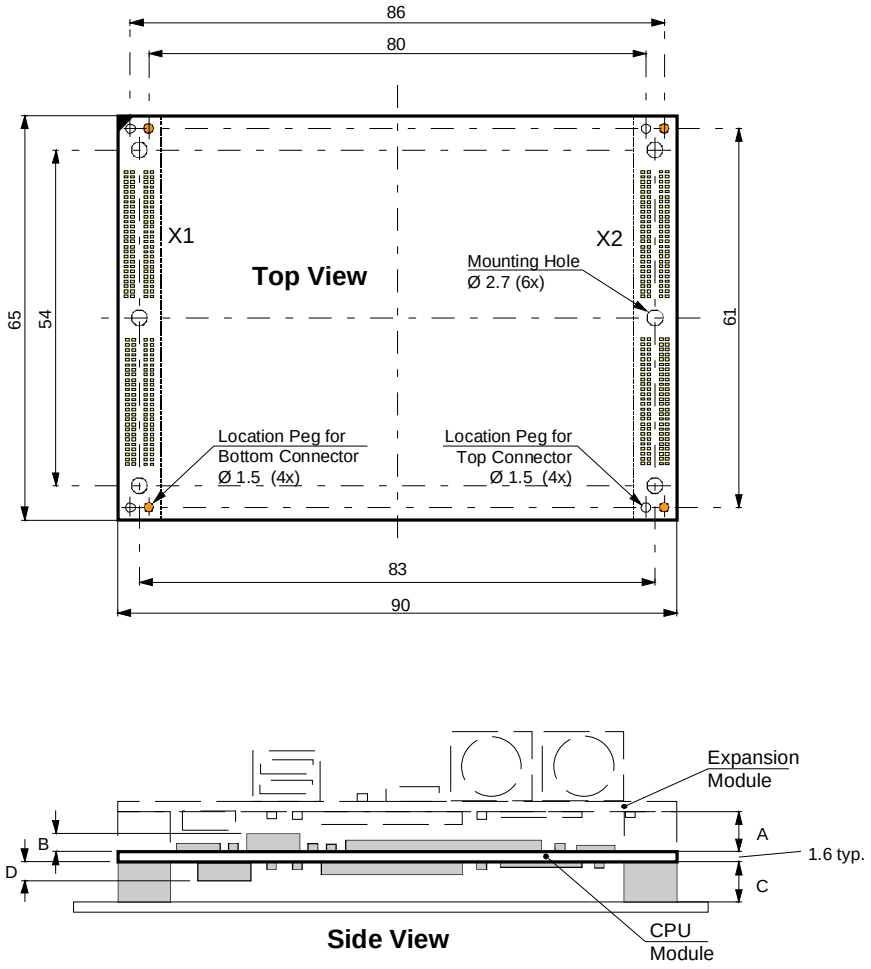
Environment

Temperature	operating	-40° .. + 85°C
	non operating	-40° .. + 85°C
Humidity (rel.)	operating	10 - 90 %
	non operating	5 - 95 %

EMI

The EXM32 Au1250 CPU Module is designed to meet DIN EN55022 (emission) and DIN EN 61000-6-2 (immunity) when mounted into in an appropriate shielded and grounded enclosure.

2.3 Mechanical Dimensions



Expansion Connector Height **A**	6.5
Top Component Height **B***	4.0
CPU Connector Height **C**	6.5
Bottom Component Height **D****	2.0

all dimensions in mm

Figure 3: EXM32-Au1250 CPU Module mechanical dimensions

2.4 Connector Positions

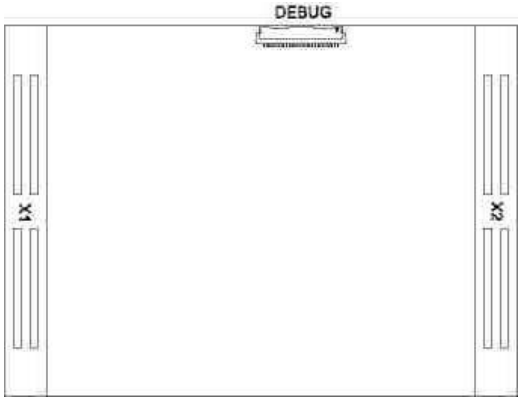


Figure 4: EXM32-AU1250 CPU-module connector positions

3 Interfaces

3.1 Connectors

3.1.1 EXM32 Connector Pin Definition

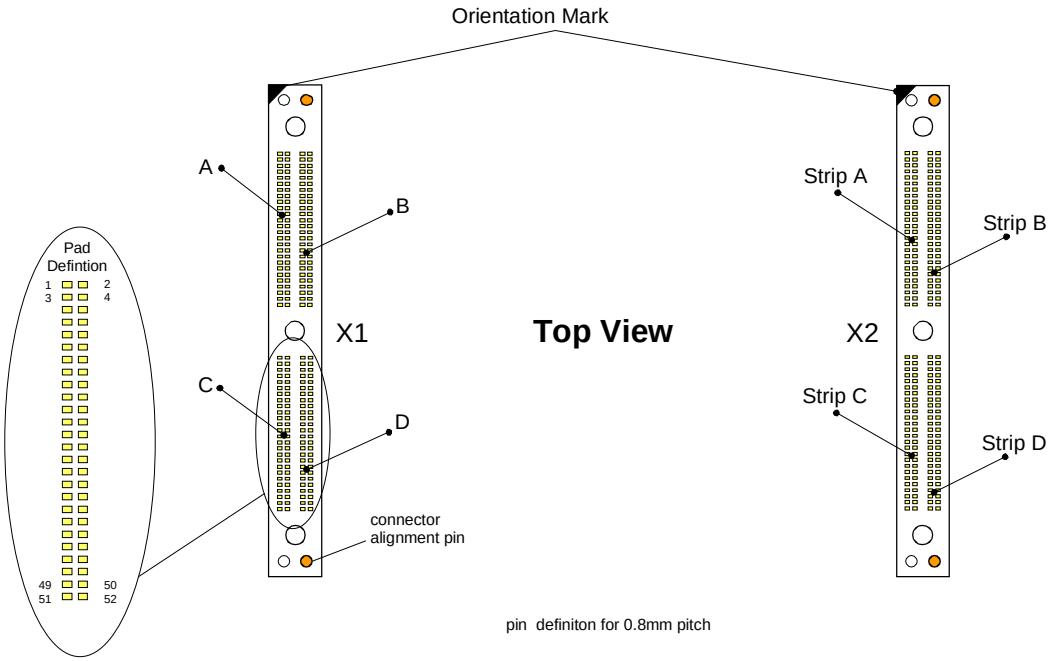


Figure 5: EXM32-Au1250 CPU-module Connectors

Note:
The EXM32 CPU Module is secured by six M2.5 screws that have to be fastened with 30 Ncm clamping torque.

3.1.2 Connector X1 (CPU Bus, Compact Flash, SPI, AC'97/I²S, PCI-E)

Strip A

Pin	Signal	Pin	Signal
1	reserved, don't use	2	CF_SCKSEL
3	reserved, don't use	4	CF_CE1#
5	reserved, don't use	6	CF_CE2#
7	CF0_PWEN	8	CF_IORD#
9	CF1_PWEN	10	CF_IOWR#
11	reserved, don't use	12	CF_POE#
13	CF0_RESET	14	CF_PWE#
15	CF1_RESET	16	CF_WAIT#
17	SPI_SS0#	18	CF_IOIS16#
19	SPI_SS1#	20	CF_PREG#
21	reserved, don't use	22	CF0_RDY_IRQ#
23	SPI_SCK	24	CF1_RDY_IRQ#
25	SPI_MOSI	26	CF0_CD#
27	SPI_MISO	28	CF1_CD#
29	GND	30	GND
31	GND	32	GND
33	GND	34	GND
35	GND	36	GND
37	GND	38	GND
39	GND	40	GND
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND
51	GND	52	GND

Strip B

Pin	Signal	Pin	Signal
1	D00	2	D01
3	D02	4	D03
5	D04	6	D05
7	D06	8	D07
9	D08	10	D09
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	D16	18	D17
19	D18	20	D19
21	D20	22	D21
23	D22	24	D23
25	D24	26	D25
27	D26	28	D27
29	D28	30	D29
31	D30	32	D31
33	BE0#	34	BE1#
35	BE2#	36	BE3#
37	IRQ_EXT1#	38	reserved, don't use
39	IRQ_EXT0#	40	CSA#
41	IRQ_MB2#	42	CSB#
43	IRQ_MB1#	44	BS#
45	IRQ_MB0#	46	OE#
47	CLK_GND	48	WE#
49	CLKOUT	50	R/W#
51	CLK_GND	52	RDY

Strip C

Pin	Signal	Pin	Signal
1	VCC3V3	2	VCC3V3
3	VCC3V3	4	VCC3V3
5	VCC3V3	6	VCC3V3
7	VCC3V3	8	VCC3V3
9	VCC3V3	10	VCC3V3
11	VCC3V3	12	VCC3V3
13	VCC3V3	14	VCC3V3STB
15	VCC3V3	16	VCC3V3STB
17	VCC3V3	18	VCC3V3STB
19	VCC3V3	20	VCC3V3STB
21	VCC3V3	22	VCC3V3STB
23	VCC3V3	24	VCC3V3STB
25	VBAT	26	VCC5V0
27	reserved, don't use	28	VCC5V0
29	PWROFF / SUSPEND	30	VCC5V0
31	SLEEP#	32	VCC5V0
33	WAKEUP	34	VCC5V0
35	PWRFLT#	36	VCC5V0
37	RESET_IN#	38	reserved, don't use
39	RESET_OUT#	40	reserved, don't use
41	AC_RESET#	42	AC'97_SDIN1
43	AC'97_SYNC/ I²S0_LRCLK	44	AC'97_SDIN0 / I²S0_SCK
45	I²S1_LRCLK	46	I²S1_SCK
47	AC_GND	48	AC'97_SDOUT / I²S0_SDIO
49	AC'97_BCLK / I²S_MCLK	50	I²S1_SDIO
51	AC_GND	52	reserved, don't use

Strip D

Pin	Signal	Pin	Signal
1	A00	2	A01
3	A02	4	A03
5	A04	6	A05
7	A06	8	A07
9	A08	10	A09
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	A16	18	A17
19	A18	20	A19
21	A20	22	A21
23	A22	24	A23
25	A24	26	A25
27	reserved, don't use	28	reserved, don't use
29	reserved, don't use	30	reserved, don't use
31	reserved, don't use	32	reserved, don't use
33	reserved, don't use	34	reserved, don't use
35	reserved, don't use	36	reserved, don't use
37	reserved, don't use	38	reserved, don't use
39	PCIE_GND	40	PCIE_GND
41	PCIE_GND	42	reserved, don't use
43	PCIE_GND	44	reserved, don't use
45	PCIE_GND	46	PCIE_GND
47	PCIE_GND	48	reserved, don't use
49	PCIE_GND	50	reserved, don't use
51	PCIE_GND	52	PCIE_GND

Connector X2 (Interfaces)

Strip A

Pin	Signal	Pin	Signal
1	FW_GND	2	reserved, don't use
3	reserved, don't use	4	reserved, don't use
5	reserved, don't use	6	reserved, don't use
7	FW_GND	8	reserved, don't use
9	reserved, don't use	10	reserved, don't use
11	reserved, don't use	12	reserved, don't use
13	FW_GND	14	JTAG_TDO
15	reserved, don't use	16	JTAG_TDI
17	reserved, don't use	18	JTAG_TCK
19	FW_GND	20	JTAG_TMS
21	reserved, don't use	22	JTAG_TRST#
23	reserved, don't use	24	CAN0_EN
25	FW_GND	26	CAN1_RX
27	reserved, don't use	28	CAN0_ERR#
29	reserved, don't use	30	CAN1_TX
31	SATA_GND	32	CAN0_STB#
33	reserved, don't use	34	CAN1_EN
35	reserved, don't use	36	CAN0_RX
37	GND	38	CAN1_ERR#
39	USB_GND	40	CAN0_TX
41	USB0(2)_D+ (3)	42	CAN1_STB#
43	USB0(2)_D- (3)	44	USB0_ID (1)
45	USB_GND	46	USB0_VBUS (1)
47	USB1(3)_D+ (3)	48	USB0(2)_PWEN
49	USB1(3)_D- (3)	50	USB1(3)_PWEN
51	USB_GND	52	USB_OC#

Strip B

Pin	Signal	Pin	Signal
1	DA_GND	2	DA_GND
3	DA0_SPDIF	4	DA1_SPDIF
5	DA_GND	6	DA_GND
7	DA0_MCLK	8	DA1_MCLK
9	DA_GND	10	DA_GND
11	DA0_SCLK	12	DA1_SCLK
13	DA0_LRCLK	14	DA1_LRCLK
15	DA0_SDIN0	16	DA1_SDOUT0
17	DA0_SDIN1	18	reserved, don't use
19	DA0_SDIN2	20	reserved, don't use
21	DA_MUTE	22	DA_ERR
23	DV_GND	24	DV_GND
25	DV0_CLK	26	DV1_CLK
27	DV_GND	28	DV_GND
29	DV0_AV#	30	DV1_AV#
31	DV0_HSYNC / DV0_SYNC	32	DV1_HSYNC / DV1_SYNC
33	DV0_VSYNC / DV0_DVALID	34	DV1_VSYNC / DV1_DVALID
35	DV_GND	36	DV_GND
37	DV0_D0	38	DV1_D0
39	DV0_D1	40	DV1_D1
41	DV0_D2	42	DV1_D2
43	DV0_D3	44	DV1_D3
45	DV0_D4	46	DV1_D4
47	DV0_D5	48	DV1_D5
49	DV0_D6	50	DV1_D6
51	DV0_D7	52	DV1_D7

(3) = USB0,1 is available on bottom pad layout, USB2,3 on top pad layout

Strip C

Pin	Signal	Pin	Signal
1	LCD_D00 (B0)	2	I2C0_SDA
3	LCD_D01 (B1)	4	I2C0_SCL
5	LCD_D02 (B2)	6	I2C1_SDA
7	LCD_D03 (B3)	8	I2C1_SCL
9	LCD_D04 (B4)	10	ETH_ACTLED#
11	LCD_D05 (B5)	12	ETH_LILED#
13	LCD_D06 (G0)	14	ETH_SPLED#
15	LCD_D07 (G1)	16	ETH_GND
17	LCD_D08 (G2)	18	ETH_TXD+ (1)
19	LCD_D09 (G3)	20	ETH_TXD- (1)
21	LCD_D10 (G4)	22	ETH_GND
23	LCD_D11 (G5)	24	ETH_RXD+ (1)
25	LCD_D12 (R0)	26	ETH_RXD- (1)
27	LCD_D13 (R1)	28	ETH_GND
29	LCD_D14 (R2)	30	reserved, don't use
31	LCD_D15 (R3)	32	reserved, don't use
33	LCD_D16 (R4)	34	VGA_GND
35	LCD_D17 (R5)	36	reserved, don't use
37	LCD_VDON	38	VGA_GND
39	LCD_M_DE	40	reserved, don't use
41	LCD_VCON	42	VGA_GND
43	LCD_HSYNC	44	reserved, don't use
45	LCD_VSYNC	46	VGA_GND
47	LCD_DON	48	reserved, don't use
49	LCD_SHFCLK	50	reserved, don't use
51	LCD_BLON	52	VGA_GND

Strip D

Pin	Signal		Pin	Signal	
	GPIO Mode	~~LCD2 Mode~~		GPIO Mode	~~LCD2 Mode~~
1	GP_IN7	not available	2	nc	not available
3	GP_IN6	not available	4	nc	not available
5	GP_IN5	not available	6	nc	not available
7	GP_IN4	not available	8	nc	not available
9	GP_IN3	not available	10	nc	not available
11	GP_IN2	not available	12	nc	not available
13	GP_IN1	not available	14	nc	not available
15	GP_IN0	not available	16	nc	not available
17	GP_OUT7	not available	18	SDIO_WP	
19	GP_OUT6	not available	20	SDIO_CLK	
21	GP_OUT5	not available	22	SDIO_CD#	
23	GP_OUT4	not available	24	SDIO_CMD	
25	GP_OUT3	not available	26	SDIO_DAT0	
27	GP_OUT2	not available	28	SDIO_DAT1/IRQ#	
29	GP_OUT1	not available	30	SDIO_DAT2/RW	
31	GP_OUT0	not available	32	SDIO_DAT3	
33	reserved, don't use		34	CPUID0 (2)	
35	MODULE_DETECT		36	CPUID1 (2)	
37	COM0_TXD		38	FR_TXD	
39	COM0_RXD		40	FR_RXD	
41	COM0_RTS#		42	FR_TXEN#	
43	COM0_CTS#		44	FR_RXEN#	
45	COM1_TXD		46	FR_BGE	
47	COM1_RXD		48	FR_EN	
49	COM1_RTS#		50	FR_STB#	
51	COM1_CTS#		52	FR_ERR#	

(1) = signal connected only to bottom pad layout (2) = signal input on bottom pad layout / signal output on top pad layout

Please note that all pins, that are marked with "reserved, don't use" **must not be used** for general purpose hardware. They may be used in specific combinations of CPU modules and motherboards.

3.2 Connector X1

3.2.1.1 Power Supply

All Signals are TTL level signals unless other specified.

N.C.	not connected
I.C.	internal connected - not to be used by customer
GND	logic ground
VCC3V3	3.3 VDC ± 5% main power supply
VCC3V3STB	3.3 VDC standby voltage (e.g. for self-refreshing SDRAM, CPU in sleep mode)
VCC5V0	5.0 VDC ± 10% optional power supply
VBAT	battery voltage (e.g. for real-time clock, battery is on EXM32 Motherboard)

3.2.1.2 SPI Bus Interface

Up to two SPI (Serial Peripheral Interface) bus channels may be provided on EXM32 CPU Modules. All signals are LV-TTL level signals.

SPI_SCK	Serial Clock output signal
SPI_MOSI	Master Output / Slave Input signal
SPI_MISO	Master Input / Slave Output signal
SPI_SS<1:0>#	Slave Select signals, active low

3.2.1.3 Compact Flash Interface

The Compact Flash interface can be used in 2 Modes: "Memory Mode" and in "I/O Mode". Address and data lines are connected the CPU bus.

CF<1:0>_CD#	These Card Detect pins are connected to GND on the Compact Flash Storage Card or CF+ Card. They are used by the host to determine that the CompactFlash Storage Card or CF+ Card is fully inserted into its socket.
CF_SCKSEL	Allows to multiplex between 2 CF-Slots (0: Slot0; 1: Slot1), glue logic is required, is an output of the EXM32 CPU Module.
CF_CE<2:1>#	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the Odd byte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1# and CE2 # allows 8 bit hosts to access all data on D0-D7.
CF_IORD#	This signal is not used in PC Card Memory Mode. in "PC Card I/O Mode" this signal is an I/O Read strobe generated by the host. It gates I/O data onto the bus from the CompactFlash Storage Card or CF+ Card when the card is configured to use the I/O interface, active low.
CF_IOWR#	This signal is not used in PC Card Memory Mode. in "PC Card I/O Mode" the I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (raising edge), active low.
CF_POE#	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers, active low.

CF<1:0>_RDY_IRQ# in PC Card Memory Mode:

In Memory Mode this signal is set high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Storage Card or CF+ Card has been powered up with +RESET continuously disconnected or asserted.

in PC Card I/O Mode:

The signal is IREQ# . After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.

CF<1:0>_RESET When the pin is high, this signal resets the CompactFlash Storage Card or CF+ Card. The CompactFlash Storage Card or CF+ Card is reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF+ Card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.

CF<1:0>_ PWEN When the pin is set high, the power supply for Compact Flash socket is enabled.

CF_PWE# in PC Card Memory Mode:

This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.

in PC Card I/O Mode:

In PC Card I/O Mode, this signal is used for writing the configuration registers only.

CF_WAIT# The WAIT# signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress.

CF_IOIS16# in PC Card Memory Mode:

Used as Write Protect signal. The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.

in PC Card I/O Mode:

When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation, the signal indicates if the selected I/O is a 16 Bit Port (IOIS16#). A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed data port.

CF_PREG# in PC Card Memory Mode:

This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.

in PC Card I/O Mode:

The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.

3.2.1.4 CPU Bus

D<31:00> CPU Data bus lines

A<25:00> CPU Address bus lines

BE<3:0># Byte Enable signals for **write cycles only**, BE0# indicates the least significant byte, active low

CSA#, CSB# Chip Select signals for external devices, active low

OE# Output Enable signal (read strobe), active low

WE# Write Enable signal (write strobe), active low

R/W# Read/Write signal for direction control of Data Bus buffers, output from CPU Module, write cycle = low

RDY Ready signal from peripheral, indicates that a transfer is complete, active high

BS# Bus Start signal, indicates the start of a bus cycle, active low

RESET_IN#	CPU Module Reset Input, active low
RESET_OUT#	This output is the system reset generated from the CPU Module to reset external devices, active low
CLKOUT	System Clock, generated from the CPU Module
CLK_GND	Clock GND, used for shielding / controlled impedance
IRQ_EXT<1:0>#	Interrupt Request from Extension Modules, active low, IRQ_EXT0# has highest priority
IRQ_MB<2:0>#	Interrupt Request from Motherboard, active low, IRQ_MB0# has highest priority
(DREQ<1:0>#)	DMA Request Inputs are used by external devices to indicate whether they need service from the CPU modules DMA controller, active low (not available on the EXM32 AU1250 CPU Module).
(DRAK<1:0>#)	DMA Request Acknowledge outputs, notifies acceptance of DMA transfer request to external device which has output DREQ#; active low (not available on the EXM32 AU1250 CPU Module).
(DACK<1:0>#)	DMA Acknowledge outputs, notification Strobe output to external device which has output DREQ#; active low. (not available on the EXM32 AU1250 CPU Module)
PWRFLT#	Module input, indicates that the primary power supply voltage of the motherboard is dropping below the operating voltage range. This signal can be used to save a limited amount of data in a non-volatile memory before the CPU shuts down or to enter sleep mode using VCC BAT.
SLEEP#	Sleep output, this signal is used to indicate the CPUs sleep mode to external devices, active low.
PWROFF/SUSPEND	Power Off/Suspend output, this signal is used to shutdown supply voltages, only VSTBY and VBAT may be available, active high.
WAKEUP	Wakeup CPU from Sleep mode, input for CPU module, active high.

3.2.1.5 Audio Codec AC'97/I²S Interface

Serial data can be received from and transmitted to an AC'97 or I²S codec, that may be mounted on the motherboard. All signals are LVTTL level signals. Up to two digital sound channels may be provided on EXM32 CPU Modules:

	I²S Mode:	**AC'97 Mode:**
AC_RESET#	Codec Reset	Codec Reset
AC'97_BCLK / I²S_MCLK	Master Clock (only master mode)	Serial Data Clock (Bit Clock)
Channel 0:		
AC'97_SYNC / I²S0_LRCLK	Left/Right Channel Select (Word Select)	Frame Sync
AC'97_SDIN0 / I²S0_SCK	Serial Bit Clock	Serial Data In (Primary Codec)
AC'97_SDIN1	no function	Serial Data In (Secondary Codec)
AC'97_SDOUT / I²S0_SDIO	Serial Data In/Out	Serial Data Out
Channel 1:		
I²S1_LRCLK	Left/Right Channel Select (Word Select)	no function
I²S1_SCK	Serial Bit Clock	no function
I²S1_SDIO	Serial Data In/Out	no function

AC_GND	Audio Codec Ground for shielding purposes

3.2.1.6 PCI Express Interface (not available on the EXM32-AU1250 CPU Module)

The PCI Express Interface is a new upcoming standard. It is a high performance general purpose I/O Interconnect defined for a wide variety of future computing and communication platforms. Key PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its bandwidth-limiting, parallel bus implementation is replaced by a highly scalable, fully serial interface. The PCI Express Interface takes advantage of recent advances in point-to-point interconnects, Switch-based technology, and packetized protocol to deliver new levels of performance and features. More information is available at www.intel.com/technology/pciexpress/ and http://www.pcisig.com/home

Contact pads for up to two PCIE connection lanes are provided in the EXM32 CPU modules specification. The **PCIE** signals are intended to serve as:

(PCIE<1:0>_PET0+)	Transmitter Signal positive (not available on EXM32-AU1250 CPU Module)
(PCIE<1:0>_PET0-)	Transmitter Signal negative (not available on EXM32-AU1250 CPU Module)
(PCIE<1:0>_PER0+)	Receiver Signal positive (not available on EXM32-AU1250 CPU Module)
(PCIE<1:0>_PER0-)	Receiver Signal negative (not available on EXM32-AU1250 CPU Module)
(PCIE<1:0>_PRSNT#)	present signal (active low) (not available on EXM32-AU1250 CPU Module)
PCIE_GND	PCIE GND for shielding / controlled impedance

3.3 Connector X2

3.3.1.1 IEEE1394 (FireWire™) (not available on the EXM32-AU1250 CPU Module)

Up to two IEEE1394 ports may be provided on EXM32 CPU Modules.

(FW_TP<1:0>A+)	Twisted-Pair A Differential-Signals pos.
(FW_TP<1:0>A-)	Twisted-Pair A Differential-Signals neg.
(FW_TP<1:0>B+)	Twisted-Pair B Differential-Signals pos.
(FW_TP<1:0>B-)	Twisted-Pair B Differential-Signals neg.
(FW_CPS)	Cable Power Status
FW_GND	IEEE1394 GND for shielding / controlled impedance

3.3.1.2 Serial ATA (not available on the EXM32-AU1250 CPU Module)

One Serial ATA port may be provided on EXM32 CPU Modules.

(SATA_TX+)	Transmitter Signal positive
(SATA_TX-)	Transmitter Signal negative
(SATA_RX+)	Receiver Signal positive
(SATA_RX-)	Receiver Signal negative
SATA_GND	SATA GND for shielding / controlled impedance

3.3.1.3 USB

Four USB ports are provided on the EXM32 AU1250 CPU Module. USB<1:0> signals are available on bottom pad layout, USB<3:2> signals are available on top pad layout., intended to be used on expansion modules.
Note: All pull-up resistors are integrated on the EXM32 CPU Module.

USB<3:0>_D+	Signal positive
USB<3:0>_D-	Signal negative
USB0_ID	USB OTG Configuration ID, High= peripheral, Low=host (signal available only on bottom pad layout)
USB0_VBUS	USB Supply Voltage, also used for OTG Session Request Protocol (signal available only on bottom pad layout)
USB<3:0>_PWEN	USB Bus Power Enable signal, active high, enables the USB ports +5V supply
USB_OC#	Overcurrent Detect Signal for the USB +5V power line from motherboard, common for two USB ports, active low
USB_GND	USB GND for shielding / controlled impedance

3.3.1.4 JTAG Interface

JTAG signals are used only for boundary scan and PLD programming.

JTAG_TDO	Data is read from external device in synchronization with a TCK signal.
JTAG_TDI	Data is sent to external device in synchronization with a TCK signal.
JTAG_TCK	Functions as the serial clock input pin stipulated in the JTAG standard (IEEE standard 1149.1).
JTAG_TMS	Mode Select input - Changing this signal determines the significance of data input via the TDI pin. Its protocol conforms to the JTAG standard.

JTAG_TRST#	JTAG Reset signal is received asynchronously with TCK signal. Asserting this signal resets the JTAG interface circuit.

3.3.1.5 MOST Media Local Bus Interface (not available on the EXM32-AU1250 CPU Module)

All signals are LV-TTL level signals.

	5-pin mode (default):	3-pin mode:
(MLB_CLK)	clock input	clock input (MLBCLK)
(MLB_SI)	signal information input	no function
(MLB_SO)	signal information output	signal information in/out (MLBSIG)
(MLB_DI)	data input	no function
(MLB_DO)	data output	data in/out (MLBDAT)

3.3.1.6 CAN

Up to two CAN Bus Interfaces are provided on EXM32 CPU Modules. All signals are LV-TTL level signals. External CAN Transceivers are required to convert the LV-TTL signals to the physical CAN interface.

CAN<1:0>_TX	CAN Bus Transmit
CAN<1:0>_RX	CAN Bus Receive
CAN<1:0>_ERR#	CAN Bus Error Flag, active low
CAN<1:0>_EN	CAN Transceiver Enable, active high
CAN<1:0>_STB#	CAN Transceiver Standby, active low

3.3.1.7 Serial Audio Interface

Up to two digital audio interfaces provided on the EXM32 CPU Modules. All signals are LV-TTL level signals.

Audio Channel 0:

DA0_SPDIF	Digital Audio signal (IEC 60958)
DA0_MCLK	Master Clock
DA0_SCLK	Serial Bit Clock
DA0_LRCLK	Left/Right Channel Select (Word Select)
DA0_SDIN0	Serial Data Input

Audio Channel 1:

DA1_SPDIF	Digital Audio signal (IEC 60958)
DA1_MCLK	Master Clock
DA_SCLK	Serial Bit Clock
DA1_LRCLK	Left/Right Channel Select (Word Select)
DA1_SDOUT0	Serial Data Output 0, contains channel 1 (Left) and channel 2 (Right) information
(DA1_SDOUT1)	Serial Data Output 1, contains channel 3 (Left Surround) and channel 4 (Right Surround) information (not available on the EXM32-AU1250 CPU Module)

(DA1_SDOUT2)	Serial Data Output 2, contains channel 5 (Center) and channel 6 (Low Frequency Effect) information (not available on the EXM32-AU1250 CPU Module)
DA_ERR	Audio Error signal
DA_MUTE	Audio Mute signal
AUDIO_GND	Digital Audio Ground for shielding purposes

3.3.1.8 Digital Video Interface

Two digital video interfaces may be provided on EXM32 CPU Modules. All signals are LV-TTL level signals.

Video Channel 0:

DV0_CLK	Video Clock signal
DV0_D<7:0>	Channel 0 data lines
DV0_EN#	Port Enable, active low
DV0_AV#	Available signal, active low
DV0_HSYNC	Horizontal Sync signal, high active
DV0_SYNC	Sync signal, indicates the start of packet, high
DV_VSYNC	Vertical Sync signal, high active
DV0_DVALID	Data Valid signal, indicates if data is valid for reading or writing, high

Video Channel 1:

DV 1_CLK	Video Clock signal
DV 1_D<7:0>	Channel 1 data lines
DV 1_EN#	Port Enable, active low
DV 1_AV#	Available signal, active low
DV 1_HSYNC	Horizontal Sync signal, high active
DV 1_SYNC	Sync signal, indicates the start of packet, high active
DV 1_VSYNC	Vertical Sync signal, high active
DV 1_DVALID	Data Valid signal, indicates if data is valid for reading or writing, high active
DV_GND	Digital Video Ground for shielding purposes

3.3.1.9 Primary LCD Port

All signals are LV-TTL level signals.

LCD_D<17:00>	Data for LCD panel
LCD_HSYNC	LCD Horizontal Sync signal
LDC_VSYNC	LCD Vertical Sync signal
LCD_SHFCLK	LCD Pixel Clock
LCD_VDON	enables Supply Voltage for Display Logic
LCD_VCON	enables Power Inverter Voltage
LCD_DON	Display On signal for STN displays
LCD_BLON	enables Backlight

	in case of STN Display:	in case of TFT Display:
LDC_M_DE	AC Bias signal (M)	LCD Data Enable (DE)

3.3.1.10 I²C Interface

Up to two I²C channels may be provided on EXM32 CPU Modules. All signals are LV-TTL level signals.

I2C<1:0>_SDA	Serial Data Input/Output signal, used to connect the CPU Modules on board I²S units
I2C<1:0>_SCL	Serial Clock Input/Output signal, reserved for Motherboard and Extension Modules I²S units

3.3.1.11 Ethernet (10/100Mbit)

The signal termination is integrated on the EXM32 CPU Module. The EXM32 Ethernet Interface is designed for use with Ethernet Magnetics.

ETH_TXD+ **ETH_TXD-**	Analog Twisted Pair - Ethernet Transmit Differential Pair. These pins transmit the serial bit stream for transmission on the Unshielded Twisted Pair (UTP) cable. Available on bottom pad layout only.
ETH_RXD+ **ETH_RXD-**	Analog Twisted Pair - Ethernet Receive Differential Pair. These pins receive the serial bit stream from the Ethernet Magnetics. Available on bottom pad layout only.
ETH_GND	Ethernet GND for shielding / controlled impedance
ETH_ACTLED#	The Activity LED pin indicates either transmit or receive activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
ETH_LILED#	The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.
ETH_SPLED#	The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.

All LED signals pull external LEDs with max. 5 mA to GND.

3.3.1.12 CRT (not available on EXM32-AU1250 CPU Module)

A standard analogue CRT interface may be provided on EXM32 CPU Modules. The 75 Ohm termination resistors are integrated on the EXM32 CPU Module.

VGA_R	Red analogue video output signal for CRT displays (not available on EXM32-AU1250 CPU Module)
VGA_G	Green analogue video output signal for CRT displays (not available on EXM32-AU1250 CPU Module)
VGA_B	Blue analogue video output signal for CRT displays (not available on EXM32-AU1250 CPU Module)
VGA_H	Horizontal sync signal: This output supplies the horizontal synchronisation pulse (not available on EXM32-AU1250 CPU Module)
VGA_V	Vertical sync signal: This output supplies the vertical synchronisation pulse (not available on EXM32-AU1250 CPU Module)
VGA_GND	VGA Ground
VGA_DDC_SCL **VGA_DDC_SDA**	Display Data Channel: the signals DDC_SCL and DDC_SDA, can be used for a DDC interface between the graphics controller chip and the CRT monitor.

All signals are LV-TTL level signals.

3.3.1.13 GPIO (LCD2 is not available on the EXM32-AU1250 CPU Module)

All signals are LV-TTL level signals.

16 I/O signals are provided by an EXM32 CPU module. These signal pins can alternatively be used as secondary LCD data signals. The usage is defined by the logic level LCD2_EN that is controlled by the EXM32 CPU Module:

(LCD2_EN)	when set to high, it enables the 2nd LCD Port on GPIO Pins: high = LCD on GPIO pins low = GPIO (default)

LCD Mode:

(LCD2_D<15:00>)	Data for LCD panel	
(LCD2_HSYNC)	LCD Horizontal Sync signal	
(LDC2_VSYNC)	LCD Vertical Sync signal	
(LCD2_SHFCLK)	LCD Pixel Clock	
(LCD2_VDON)	enables Supply Voltage for Display Logic	
(LCD2_VCON)	enables Power Inverter Voltage	
(LCD2_DON)	Display On signal for STN displays	
(LCD2_BLON)	enables Backlight	
	in case of STN Display:	**in case of TFT Display:**
(LDC2_M_DE)	AC Bias signal (M)	LCD Data Enable (DE)

GPIO Mode:

GP_IN<7:0>	General Purpose Input signals for EXM32 CPU Module
GP_OUT<7:0>	General Purpose Output signals for EXM32 CPU Module

3.3.1.14 MultiMedia Card / Secure Digital Memory Card/Secure Digital Input/Output Card

A MultiMedia / Secure Digital Memory / Secure Digital Input/Output Card interface may be provided. All signals are LV-TTL level signals.

SDIO_DAT0	Bidirectional data line 0 (4-bit and 1-bit mode)
SDIO_DAT1/IRQ#	Bidirectional data line 1 (4-bit mode), interrupt signal (1-bit mode, only SDIO Card, low active)
SDIO_DAT2/RW	Bidirectional data line 2 (4-bit mode), read wait signal (1-bit mode, only SDIO Card, optional)
SDIO_DAT3	Bidirectional data line 3 (4-bit mode)
SDIO_CLK	Host to card clock signal
SDIO_CMD	Bidirectional command / response signal
SDIO_WP	Write protect, active high

SDIO_CD#	Card detect, active low

3.3.1.15 Serial Ports

All signals are LV-TTL level signals. External drivers are required to convert the LV-TTL signals to the desired physical interface like RS232, RS422, RS485.

COM0_TXD	Transmitter serial data output from serial port
COM0_RXD	Receiver serial data input
COM0_CTS#	handshake signal which notifies the UART that the modem is ready to receive data
COM0_RTS#	handshake signal which notifies the modem that the UART is ready to receive data
COM1_TXD	Transmitter serial data output from serial port
COM1_RXD	Receiver serial data input
COM1_CTS#	handshake signal which notifies the UART that the modem is ready to receive data
COM1_RTS#	handshake signal which notifies the modem that the UART is ready to receive data

3.3.1.16 FlexRay (not available on the EXM32-AU1250 CPU Module)

A FlexRay interface is provided on EXM32 CPU Modules. All signals are LV-TTL level signals. An external transceiver is required to convert the LV-TTL signals to the desired physical interface.

(FR_TXD)	transmit data
(FR_RXD)	receive data
(FR_TXEN#)	transmitter enable, active low
(FR_RXEN#)	receive data enable, active low
(FR_BGE)	bus guardian enable
(FR_EN)	transceiver enable, active high
(FR_STB#)	transceiver standby, active low
(FR_ERR#)	bus error flag, active low

3.3.1.17 MISC

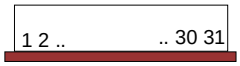
MODULE_DETECT	A lower EXM32 Module can detect if another Module is mounted on top, this feature is used for automatic JTAG chain configuration: a) the pad on every modules bottom side is connected to VCC3V3 b) the top side pad is used for readout - there is no connection to the bottom side pad!
CPUID<1:0>	There are no direct connections between the top and bottom side pads of CPUID<1:0>! The modules ID value (binary) is available on the top side signal pads for the next upper Module. The ID value is generated by reading the lower module's ID value vie the bottom side pads and incrementing this value by 1. A EXM32 motherboard has the ID value '00', the CPU Module ID value is '01', … As a second function, the module ID value may be used to address the modules/motherboards ID-EEPROM on the I²C Bus, refer to.

3.4 Debug Connector

The Debug Connector accepts a FPC cable, Channel 0 connects the debug adaptor to the on board PLDs (FPGA,CPLD) and Channel 1 to the CPUs JTAG Debug Port. The on board PLDs (FPGA,CPLD) can be accessed via the debug adaptor or the EXM32 Connector.

DEBUG

31 Pin FPC Connector, RM0.50, 90°, Bottom contact
Weitronic 570-31-30-(10)



Pin	Signal
1	VCC
2	VCCIO
3	TCK0
4	TRST0#
5	TDI0
6	TDO0
7	TMS0
8	SRESET#
9	GND
10	TCK1
11	TRST1#
12	TDI1
13	TDO1
14	TMS1
15	ASEBRK#
16	GND
17	TRACECLK (nc)
18	TRACESYNC (nc)
19	GND
20	TRACEDATA0 (nc)
21	TRACEDATA1 (nc)
22	TRACEDATA2 (nc)
23	TRACEDATA3 (nc)
24	TRACEDATA4 (nc)
25	TRACEDATA5 (nc)
26	TRACEDATA6 (nc)
27	TRACEDATA7 (nc)
28	DEBUG DETECT
29	TXD (nc)
30	RXD (nc)
31	BOOT# (nc)

4 Hardware Description

4.1 Functional Blocks

4.1.1 CPU

The EXM32-Au1250 CPU module is equipped with the Au1250 processor. The user can choose to run the CPU at three different frequencies per option of assembly. The chosen CPU speed determines the maximum peripheral clock frequency available on the EXM32-Connector (X1B_CLKOUT).

CPU Speed	AU1250 CLKOUT (EXM32-Connector)
336 Mhz	56 Mhz
396 Mhz	66Mhz
492 Mhz	61,5Mhz
600 Mhz	66,67Mhz

Clocks

There are three crystal oscillators populated on the EXM32-AU1250. A 12 MHz crystal oscillator is feed to the AU1250 for generation of internal and external frequencies. A 25.000 MHz crystal oscillator provides the clock for a phase-locked loop (PLL) clock generator.

PLL clock generator CY22393

The PLL clock synthesiser populated on the CPU module generates the clocks for all peripheral modules..
The Cypress CY22393 clock generator features three independent phase-locked loops. The device is in-system serial and flash programmable, thus all frequency settings can be changed.
On the EXM32-SHAu1250 CPU module, the PLL clock generator is connected to Channel 0 of the integrated I²C-Bus. To access the PLL, device address 1101001 must be used.

PLL device address:	1101001x (0xD2)

The CY22393 clock generator provides up to six output clocks:

OUTPUT	FREQUENCY	MODULE CLOCK
XBUF	25.000 MHz	Ethernet Clock
CLKA	variable (default: 33.33 MHz)	Digital Video Clock
CLKB	2.000 MHz	VRG synchronisation clock
CLKC	27.000 MHz	Digital Video clock/ HSDI clock
CLKD	14.769231 MHz	Not Used
CLKE	48 Mhz	USB clock

The Cypress clock generator offers power saving features that are controlled by a programmable logic device (FPGA). The input pin SHUTDOWN#/OE three-states all outputs, when pulled LOW. If shutdown is enabled, a LOW on this pin disables all phase-locked loops, counters, the reference oscillator and all other active components. The S2/SUSPEND# connected to the SUSPEND signal input of the clock generator can be configured to shut down a customisable set of outputs and/or phase-locked loops, when LOW. This feature can be used for power saving.

For a detailed description of the PLL clock generator device please refer to the Cypress CY22393 Datasheet.

I²C ID-EEPROM

The ID-EEPROM is used to store module specific parameters. For a parameter overview and a memory map of the ID-EEPROM please refer to appendix A.
The Catalyst Supervisor CAT1026 device used on the board provides 2048 byte of serial electrical erasable and programmable read-only memory and is equipped with a two wire interface (I²C). On the EXM32-Au1250 CPU Module, the CAT1026 is connected to Channel 0 of the integrated I²C-Bus. To access the ID-EEPROM, device address 1010000 must be used.

ID-EEPROM device address:	1010000x (0xA0)

For a detailed description of the ID-EEPROM device please refer to the Catalyst CAT1026 Datasheet.

Real Time Clock

The EXM32-Au1250 CPU Module is equipped with a discrete RTC device. This module is a serial interface real time clock with built-in crystal oscillator. The Seiko Epson RTC-8564NB real time clock module offers many functions such as calendar clock, alarm, timer and frequency output (1 Hz, 32 Hz, 1024 Hz, 32.768 kHz).
The device functions can be controlled by a two wire interface (I²C). On the EXM32-Au1250 CPU Module, the RTC is connected to channel 0 of the integrated I²C-Bus.
To access the real time clock module, device address 1010001 must be used.

RTC device address:	1010001x (0xA2)

For a detailed description of the real time clock module please refer to the Seiko Epson RTC-8564NB Application Manual.

4.1.2 MMC/SD/SDIO

MultiMedia Card (MMC)/
Secure Digital Memory Card (SD)/
Secure Digital Input/Output Card (SDIO)

The EXM32-Au1250 CPU Module supports a SD/SDIO/MMC I/O Card interface.

Secure Digital Memory Card support a mechanical write protect switch. An input of the programmable logic device (FPGA) is used to readout the status of this switch. When the signal EXT_SDIO_WP is LOW, the SD Card is fully accessible. The card is write-protected, when EXT_SDIO_WP is HIGH. To readout the actual status of the write protect switch, access to the internal registers of the FPGA is necessary. The device driver must support this feature. BRDSTAT Board Status Register.

4.1.3 PC-Card/Compact Flash Interface

The EXM32-Au1250 CPU Module features a PC-Card/Compact Flash interface. This interface supports two sockets. A signal CF_SCKSEL on the EXM32 connector is used to multiplex between the two sockets 0 and 1. When CF_SCKSEL is low, socket 0 is active. Socket 1 is active, when CF_SCKSEL is HIGH. CF_SCKSEL is generated by a programmable logic device (Lattice CPLD). The reset signals CF<1:0>_RESET (active high) are generated by the programmable logic device. To reset the PC-Card/Compact Flash Card, access to the internal registers of the CPLD is necessary. The device driver must support this feature.

4.1.4 Linear Flash

Flash Memory is used for program and data storage. The EXM32 Module supports up to 128 MByte flash memory, provided by one device (see memory map). Linear Flash memory is mapped into Area 0 and 3 of the external memory space. This allows the system to boot from flash. The Linear Flash shares memory space with the Ethernet Controller, the USB Controller, the UART, two I2C-controller, the SPI-Controller, the CAN-Controller the programmable logic device (FPGA).

The EXM32 CPU Module supports write protection for Linear Flash Memory. An output of the programmable logic device (FPGA) is used to enable or disable the write protection (shared with NAND Flash write protection). When the output is HIGH, the Flash Memory is fully accessible. The card is write-protected, when the programming voltage is turned off. The programming voltage is disabled, when the output is LOW. To enable or disable the write protection, access to the internal registers of the FPGA is necessary. The device driver must support this feature.

For detailed description of the memory space mapping please refer to chapter 6.2 "Off-chip Memory Map".

4.1.5 NAND-Flash

The Au1250 CPU module is availabel with a optional 8 Bit NAND Flash assembly.
The EXM32 CPU Module supports write protection for NAND-Flash Memory. When the output is HIGH, the Flash Memory is fully accessible. The card is write-protected, when the output is LOW. To enable or disable the write protection, access to the internal registers of the FPGA is necessary. The device driver must support this feature.

4.1.6 DDR2-SDRAM

The EXM32-Au1250-CPU Module provides up to 256 Mbyte DDR2-SDRAM.
The CPU Module uses two DDR2-banks, each bank with two memory modules.
Each memory module is organised x16-bit, in order to provide the 32-bit wide working memory, directly interfaced to the CPU. All SDRAM signals are driven directly by the processor. For detailed description of the memory space mapping and for detailed setup and initialization of the Au1250 SDRAM Controller please refer to chapter 6.2 "Off-chip Memory Map".

4.1.7 Ethernet

The EXM32-Au1250 CPU Module is equipped with an SMSC LAN91C111I Single Chip MAC + PHY, to support 10/100BaseT Ethernet.
Power saving modes can be controlled individually for the MAC and the PHY by software.
The Ethernet Controller I/O space is mapped into Area 0 and 3 of the external memory space. The SMSC LAN91C111I shares its I/O space with the Flash Memory, the USB Controller and the programmable logic device (FPGA).
For detailed description of the memory space mapping please refer chapter 6.2 "Off-chip Memory Map". For a detailed description of the Ethernet Controller please refer to the SMSC LAN91C111I Datasheet.

4.1.8 USB

The Au1250 microprocessor features two integrated USB 2.0 high speed ports. A 2.0 compatible enhanced host controller and and a 2.0 compatible USB device with OTG support. The USB host controller of the Au1250 processor is connected to port 1, the device controller to port 0 of the EXM32-Au1250 CPU Module.

An external power switch and over-current detection is implemented in a programmable device (FPGA). The Power Enable for USB Port 0 and 1 can be set in the peripheral devices control register (PDCTRL). The status of the overcurrent is available in the board status register (BRDSTAT). 6.1.7 PDCTRL Peripheral Devices Control Register.

For a detailed description of the integrated USB controller please refer to Au1250 Datasheet.

4.1.9 Graphics Controller

4.1.9.1 Integrated Graphics Controller

The Au1250 features an integrated LCD Controller with a maximum resolution of 2048x2048 pixel. This controller is capable of driving 4-24 bit color STN and TFT displays. If 24-Bit Interface is necessary additional 6 Bit of the LCD 2 Interface have to be used. In this case no GPIO function is available on the EXM Connector. Refer to Table 6 and section 5.1.12 GPIO Interface for details.

The Au1250 CPU Module provides four signals used to control display power sequences:

Signal	TYPE	INIT	SIGNAL	DESCRIPTION
X1C_LCD2_VDON	O	0	VDON	enables digital power supply
X1C_LCD2_VCON	O	0	VCON	enables power inverter voltage
X1C_LCD2_BLON	O	0	BLON	Enables backlight inverter
X1C_LCD2_DON	O	0	DON	enables display (only STN/D-STN Displays)*

* connect to pin DISP_OFF# on STN/D-STN displays

Software controlls the timing for the LCD power up seqence. The LCD power control signals can be set in the LCD Control Register. Refer to section 6.1.5 LCDCTRL LCD Control Register for details.

LCD power-supply control sequence:

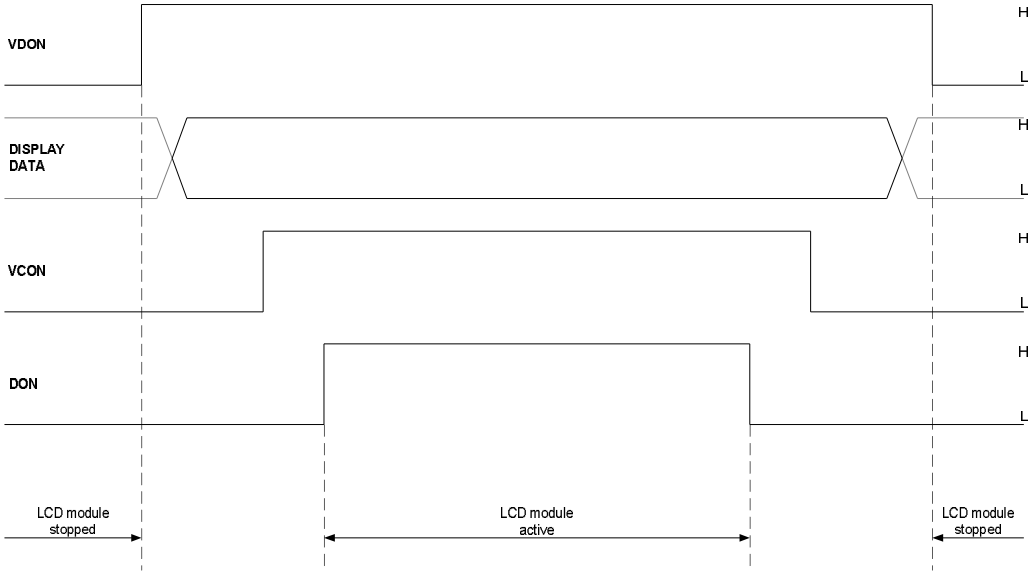


Figure 6: EXM32-Au1250 CPU-module LCD power-on timing

For valid timing values please refer to the display manufacturer's datasheet.

The AU1250 LCD interface is connected to the EXM32-Connector as follows.

LCD Signal	Mono STN Panel		Color STN Panel		Color TFT Panel			EXM32-Connector Signals
	4-bit	8-bit	Single	Dual	12-bit	18-bit	24-bit	
LCD_D[0]	M0	M0	D0	D0			B0	GP_OUT[2]/LCD2_D[13]
LCD_D[1]	M1	M1	D1	D1			B1	GP_OUT[3]/LCD2_[D12]
LCD_D[2]	M2	M2	D2	D2		B0	B2	LCD_B[0]
LCD_D[3]	M3	M3	D3	D3		B1	B3	LCD_B[1]
LCD_D[4]		M4		D4	B0	B2	B4	LCD_B[2]
LCD_D[5]		M5		D5	B1	B3	B5	LCD_B[3]
LCD_D[6]		M6		D6	B2	B4	B6	LCD_B[4]
LCD_D[7]		M7		D7	B3	B5	B7	LCD_B[5]
LCD_D[8]							G0	GP_OUT[4]/LCD2_D[11]
LCD_D[9]							G1	GP_OUT[5]/LCD2_[D10]
LCD_D[10]						G0	G2	LCD_G[0]
LCD_D[11]						G1	G3	LCD_G[1]
LCD_D[12]					G0	G2	G4	LCD_G[2]
LCD_D[13]					G1	G3	G5	LCD_G[3]
LCD_D[14]					G2	G4	G6	LCD_G[4]
LCD_D[15]					G3	G5	G7	LCD_G[5]
LCD_D[16]							R0	GP_OUT[6]/LCD2_D[9]
LCD_D[17]							R1	GP_OUT[7]/LCD2_D[8]
LCD_D[18]						R0	R2	LCD_G[0]
LCD_D[19]						R1	R3	LCD_G[1]
LCD_D[20]					R0	R2	R4	LCD_G[2]
LCD_D[21]					R1	R3	R5	LCD_G[3]
LCD_D[22]					R2	R4	R6	LCD_G[4]
LCD_D[23]					R3	R5	R7	LCD_G[5]
LCD_BIAS								LCD_M_DE
LCD_FCLK								LCD_VSYNC
LCD_LCLK								LCD_HSYNC
LCD_PCLK								LCD_SHFCLK

Table 6: EXM32-Au1250 LCD-Interface

4.1.9.2 Spread Spectrum LCD Clock Modulator

The AU1250 CPU Module is equiped with a DS1081L Clock Modulator.
The AU1250 LCD Clock can be feed through the DS1081L for EMV purposes or bypassed by an analog switch. Refer to section 6.1.5 LCDCTRL LCD Control Register and the Maxim DS1081L datasheet for details.

4.1.10 Camera Interface

The LCD 2 interface, available at the EXM32-connector, is directly connected to the Au1250 CPU Camera Interface (8-bit data). For details refer to the AU1250 Datasheet.

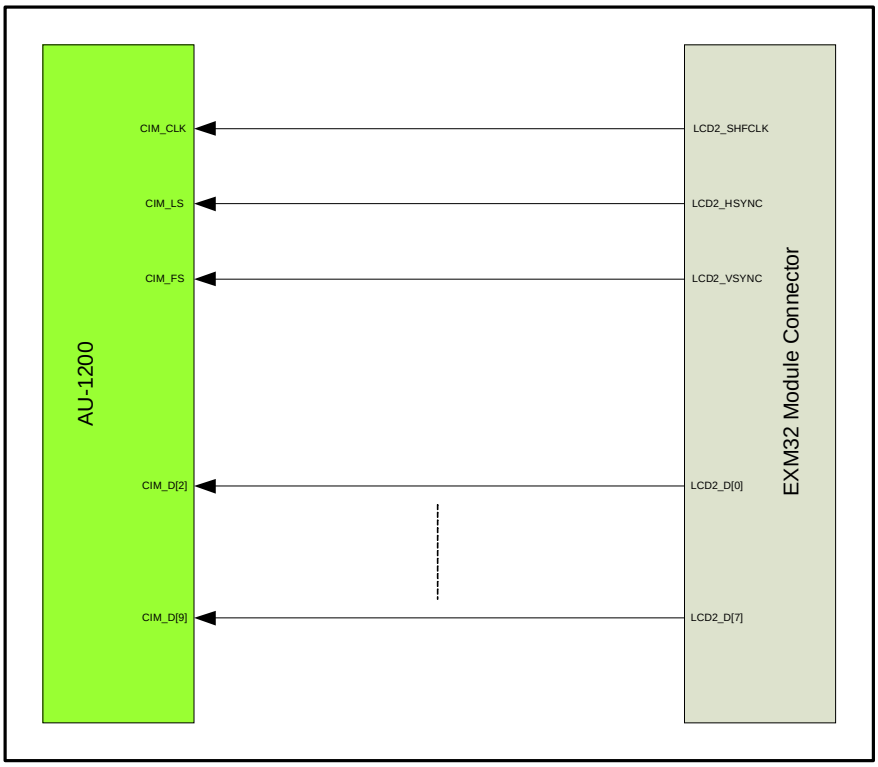


Figure 7: EXM32-AU1250 CPU-module camera interface

EXM32 Connector	Camera Interface Signal
LCD2_D[0]/GP_IN[7]	CIM_D2
LCD2_D[1]/GP_IN[6]	CIM_D3
LCD2_D[2]/GP_IN[5]	CIM_D4
LCD2_D[3]/GP_IN[4]	CIM_D5
LCD2_D[4]/GP_IN[3]	CIM_D6
LCD2_D[5]/GP_IN[2]	CIM_D7
LCD2_D[6]/GP_IN[1]	CIM_D8
LCD2_D[7]/GP_IN[0]	CIM_D9

4.1.11 GPIO-/(LCD2) Interface (V0.5 Update)

The AU1250 LCD2 Interface can be used either in LCD2 or GPIO mode. The Camera Interface of the AU1250 CPU is directly connected to the dual function pins LCD2_D[7:0]/GP_IN[7:0] on the EXM Connector. Refer to the AU1250 Datasheet to set these pins in GPIN Mode if necessary. The MSB of the LCD2 Interface LCD2_D[8:15]/ GP_OUT[7:0] can be used either in GPOUT Mode or in LCD Mode. If 24-Bit TFT Mode on LCD 1 Interface is necessary, the LCD 2 interface is used to provide the additional 6 Bit to the EXM Connector (see Table 6)

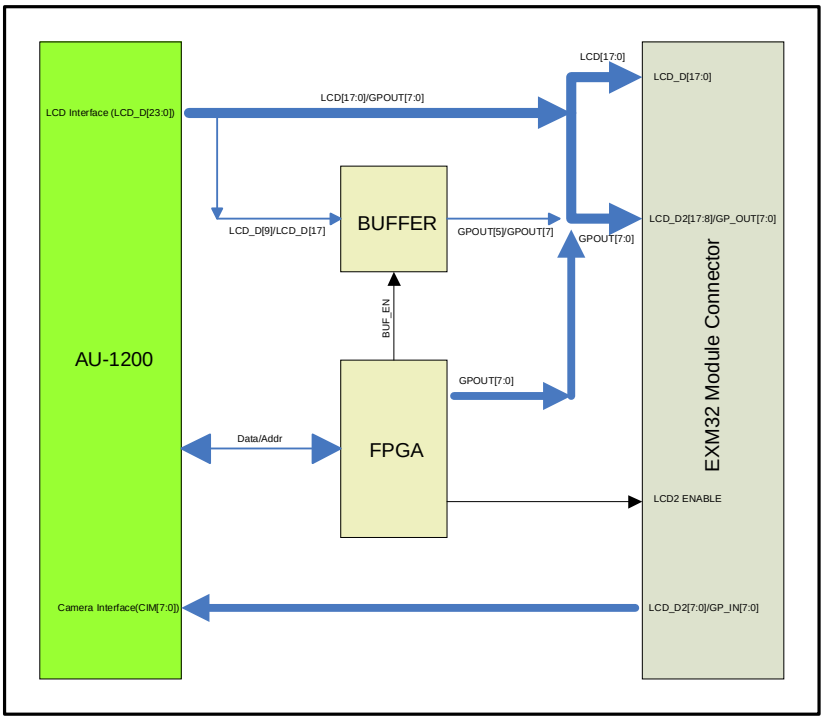


Figure 8: EXM32-LCD2-Interface

To set the LCD Interface in GPIO Mode reset Bit 5 in BRDCTRL Resister (6.1.3 BRDCTRL Board Control Register). Signal LCD2_ENABLE reflects the Status of Bit 5 to the EXM Connector. It can be used to control external buffers on the Motherboard. If LCD mode is disabled the GPOUT Register (Baseaddress 0x3FFF_003C) takes control of the Signals LCD2_D[8:15]/ GP_OUT[7:0]. Refer to section 6.1.16 GPOUT General Purpose Output Register.

LCD Mode BRD_CTRL[5]=LCD2_EN=0 Baseaddress=0x3FFF0008	**GPIO Mode** BRD_CTRL[5]=LCD2_EN=1 Baseaddress=0x3FFF0008	**EXM32 Connector Signals**
AU1250 CIM[D9 :D2]/GPIO[209:202] (Refer to AU1250 Datasheet to set these pins to Camera Interface Mode)	AU1250 CIM[D9 :D2]/GPIO[209:202] (Refer to AU1250 Datasheet to set these pins to GPIN Mode)	GPI[7:0]/LCD2_D[7:0]
AU1250 LCD2[17] (24-Bit-TFT)	GPOUT[7] (Baseaddress=0x3FFF003C)	GPO[7]/LCD2_D[8]
AU1250 LCD_D[16]/GPIO[211] (24-Bit-TFT)	GPOUT[6 (Baseaddress=0x3FFF003C)	GPO[6]/LCD2_D[9]

AU1250 LCD_D[9] (24-Bit-TFT)	GPOUT[5] (Baseaddress=0x3FFF003C)	GPO[5]/LCD2_D[10]
AU1250 LCD_D[8]/GPIO[210] (24-Bit-TFT)	GPOUT[4] (Baseaddress=0x3FFF003C)	GPO[4]/LCD2_D[11]
AU1250 LCD_D[1]/GPIO[201] (24-Bit-TFT)	GPOUT[3] (Baseaddress=0x3FFF003C)	GPO[3]/LCD2_D[12]
AU1250 LCD_D[0]/GPIO[200] (24-Bit-TFT)	GPOUT[2] (Baseaddress=0x3FFF003C)	GPO[2]/LCD2_D[13]
Not used	GPOUT[1] (Baseaddress=0x3FFF003C)	GPO[1]/LCD2_D[14]
Not used	GPOUT[0] (Baseaddress=0x3FFF003C)	GPO[0]/LCD2_D[15]

Table 7: Signal routing in LCD2-/GPIO-Mode

4.1.12 CAN Bus

The EXM32-AU1250 CPU Module features two independent OKI ML9620 CAN bus controllers. The operation mode of the CAN transceivers (on an EXM32-Motherboard) is controlled by the signals CAN<1:0>_EN and CAN<1:0>_STB#. Those signals can be controlled in peripheral devices control register (PDCTRL, section 6.1.7) in the FPGA.

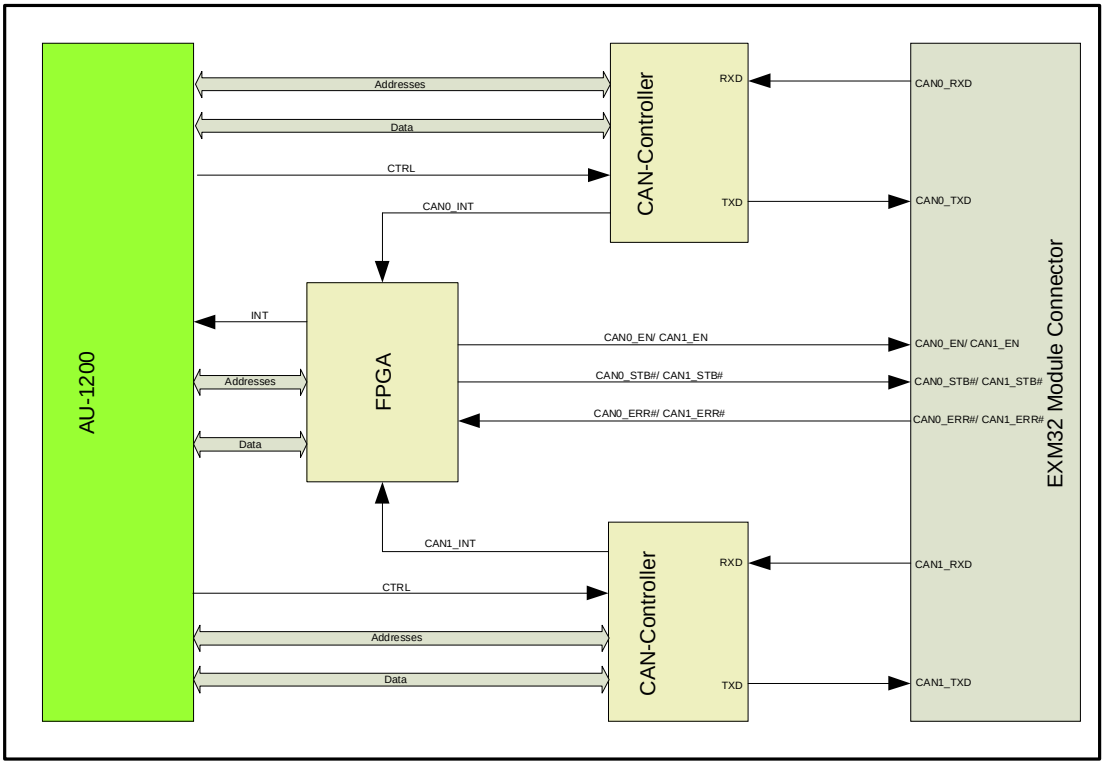


Figure 8: EXM32-Au1250 CAN interface

4.1.13 Serial Communication Interfaces (COM0,COM1)

The EXM32-AU1250 CPU module features a two channel serial communication Interface.

COM0: The Au1250 integrated serial interface 1 is connected to the EXM32 Connector . The second serial interface (PSC1) of the AU1250 is not used. Refer to the AU1250 datasheet for a detailed description of the AU1250 integrated UART.

COM1: COM1 is implemented in an FPGA. The FPGA integrated IP is a 16550 compatible UART. The 8 bit interface of the UART is connected to the lower 8 bit of the external 16 bit data bus of the Au1250-CPU Module.

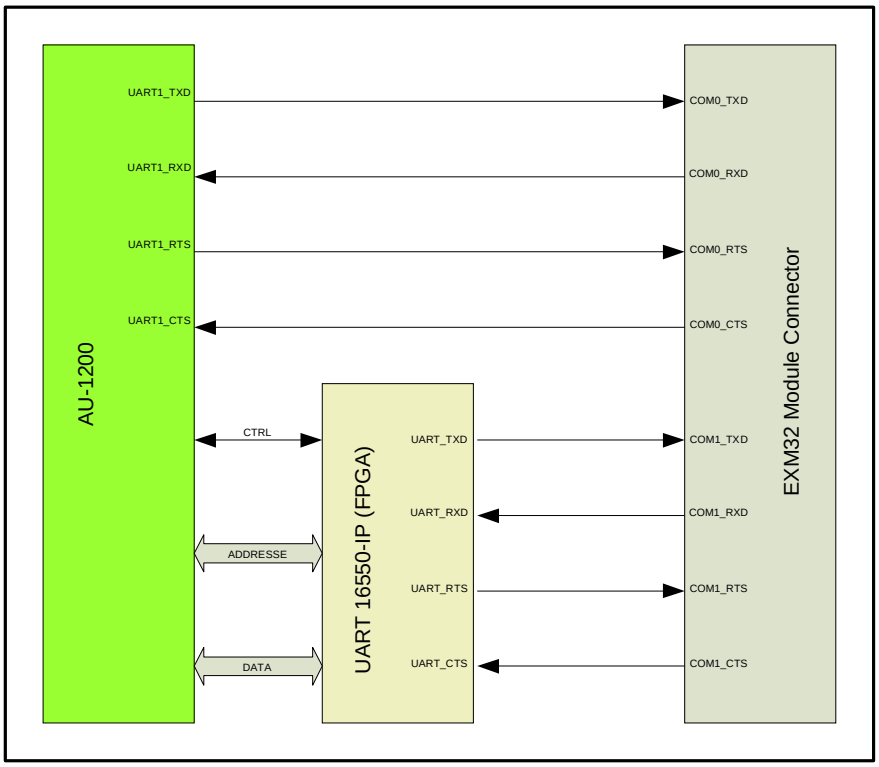


Figure 9: EXM32- Au1250 serial interfaces

4.1.13.1 UART Clock (COM1)

The FPGA integratet UART uses the AU1250 CLOCKOUT. Refer to chapter 5.1 for details.

Name	Source	Min	Max	Resolution	Description
clk	CPU	14.0625 bps	115200 bps		UART Clock

4.1.13.2 Registers of the FPGA integrated UART (COM1)

Base Address: 0x1FFF4000/0x3FFF4000

Name	Address	Width	Access	Description
Receiver Buffer	0	8	R	Receiver FIFO output
Transmitter Holding Register (THR)	0	8	W	Transmit FIFO input
Interrupt Enable	1	8	RW	Enable/Mask interrupts generated by the UART
Interrupt Identification	2	8	R	Get interrupt information
FIFO Control	2	8	W	Control FIFO options
Line Control Register	3	8	RW	Control connection
Modem Control	4	8	W	Controls modem
Line Status	5	8	R	Status information
Modem Status	6	8	R	Modem Status

In addition, there are 2 cascaded 8-bit clock dividers.
The registers can be accessed when the 7th (DLAB) bit of the Line Control Register is set to '1'. At this time the above registers at addresses 0-1 can't be accessed.

Name	Address	Width	Access	Description
Divisor Latch Byte 1 (LSB)	0	8	RW	The LSB of the divisor latch
Divisor Latch Byte 2	1	8	RW	The MSB of the divisor latch

4.1.13.2.1 Interrupt Enable Register (IER)

This register allows enabling and disabling interrupt generation by the UART.

Bit #	Access	Description
0	RW	Received Data available interrupt '0' – disabled '1' – enabled
1	RW	Transmitter Holding Register empty interrupt '0' – disabled '1' – enabled
2	RW	Receiver Line Status Interrupt '0' – disabled '1' – enabled
3	RW	Modem Status Interrupt '0' – disabled '1' – enabled
7-4	RW	Reserved. Should be logic '0'.

Table 7: External UART Interrupt Enable Register (IER)

Reset Value: 00h

4.1.13.2.2 Interrupt Identification Register (IIR)

The IIR enables the programmer to retrieve what is the current highest priority pending interrupt.
Bit 0 indicates that an interrupt is pending when it's logic '0'. When it's '1' – no interrupt is pending.
The following table displays the list of possible interrupts along with the bits they enable, priority, and their source and reset control.

Bit 3	**Bit 2**	**Bit 1**	**Priority**	Interrupt Type	**Interrupt Source**	**Interrupt Reset Control**
0	1	1	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the Line Status Register
0	1	0	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
1	1	0	2nd	Timeout Indication	There's at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 Char times.	Reading from the FIFO (Receiver Buffer Register)
0	0	1	3rd	Transmitter Holding Register empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR.
0	0	0	4th	Modem Status	CTS, DSR, RI or DCD.	Reading the Modem status register.

Bits 4 and 5: Logic '0'.
Bits 6 and 7: Logic '1' for compatibility reason.

Reset Value: C1h

4.1.13.2.3 FIFO Control Register (FCR)

The FCR allows selection of the FIFO trigger level (the number of bytes in FIFO required to enable the Received Data Available interrupt). In addition, the FIFOs can be cleared using this register.

Bit #	Access	Description
0	W	Ignored (Used to enable FIFOs in NS16550D). Since this UART only supports FIFO mode, this bit is ignored.
1	W	Writing a '1' to bit 1 clears the Receiver FIFO and resets its logic. But it doesn't clear the shift register, i.e. receiving of the current character continues.
2	W	Writing a '1' to bit 2 clears the Transmitter FIFO and resets its logic. The shift register is not cleared, i.e. transmitting of the current character continues.
5-3	W	Ignored
7-6	W	Define the Receiver FIFO Interrupt trigger level '00' – 1 byte '01' – 4 bytes '10' – 8 bytes '11' – 14 bytes

Reset Value : 11000000b

4.1.13.2.4 Line Control Register (LCR)

The line control register allows the specification of the format of the asynchronous data communication used. A bit in the register also allows access to the Divisor Latches, which define the baud rate. Reading from the register is allowed to check the current settings of the communication.

Bit #	Access	Description
1-0	RW	Select number of bits in each character '00' – 5 bits '01' – 6 bits '10' – 7 bits '11' – 8 bits
2	RW	Specify the number of generated stop bits '0' – 1 stop bit '1' – 1.5 stop bits when 5-bit character length selected and 2 bits otherwise Note that the receiver always checks the first stop bit only.
3	RW	Parity Enable '0' – No parity '1' – Parity bit is generated on each outgoing character and is checked on each incoming one.
4	RW	Even Parity select '0' – Odd number of '1' is transmitted and checked in each word (data and parity combined). In other words, if the data has an even number of '1' in it, then the parity bit is '1'. '1' – Even number of '1' is transmitted in each word.
5	RW	Stick Parity bit. '0' – Stick Parity disabled '1' - If bits 3 and 4 are logic '1', the parity bit is transmitted and checked as logic '0'. If bit 3 is '1' and bit 4 is '0' then the parity bit is transmitted and checked as '1'.
6	RW	Break Control bit '1' – the serial out is forced into logic '0' (break state). '0' – break is disabled
7	RW	Divisor Latch Access bit. '1' – The divisor latches can be accessed '0' – The normal registers are accessed

Reset Value: 00000011b

4.1.13.2.5 Modem Control Register (MCR)

The modem control register allows transferring control signals to a modem connected to the UART.

Bit #	Access	Description
0	W	Data Terminal Ready (DTR) signal control '0' – DTR is '1' '1' – DTR is '0'
1	W	Request To Send (RTS) signal control '0' – RTS is '1' '1' – RTS is '0'
2	W	Out1. In loopback mode, connected Ring Indicator (RI) signal input
3	W	Out2. In loopback mode, connected to Data Carrier Detect (DCD) input.
4	W	Loopback mode '0' – normal operation '1' – loopback mode. When in loopback mode, the Serial Output Signal (STX_PAD_O) is set to logic '1'. The signal of the transmitter shift register is internally connected to the input of the receiver shift register. The following connections are made: DTR ➔ DSR RTS ➔ CTS Out1 ➔ RI Out2 ➔ DCD
5	W	RTS/CTS Autoflow. '0' -RTS/CTS is exclusively controled by software. (Set RTS bit in modem control register mcr[1], Read CTS bit in the modem status register mcr[0/4]) '1' –RTS/CTS is controled by hardware, but can be set or read by software as well. - RTS is set as soon as the trigger level is reached and reset as soon as the trigger level is underflown. - If CTS is set, the transmission of a full transmitt-fifo is interrupted immediately and will be continued at the point of interruption if CTS is reset. Software can take take control on the hardware-handshake in addition, if autoflow is selected.
7-6	W	Ignored

Reset Value: 0

4.1.13.2.6 Line Status Register (LSR)

Bit #	Access	Description
0	R	Data Ready (DR) indicator. '0' – No characters in the FIFO '1' – At least one character has been received and is in the FIFO.
1	R	Overrun Error (OE) indicator '1' – If the FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No overrun state
2	R	Parity Error (PE) indicator '1' – The character that is currently at the top of the FIFO has been received with parity error. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt.

Bit #	Access	Description
		'0' – No parity error in the current character
3	R	Framing Error (FE) indicator '1' – The received character at the top of the FIFO did not have a valid stop bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No framing error in the current character
4	R	Break Interrupt (BI) indicator '1' –A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character (start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. Generates Receiver Line Status interrupt. '0' – No break condition in the current character
5	R	Transmit FIFO is empty. '1' – The transmitter FIFO is empty. Generates Transmitter Holding Register Empty interrupt. The bit is cleared when data is being been written to the transmitter FIFO. '0' – Otherwise
6	R	Transmitter Empty indicator. '1' – Both the transmitter FIFO and transmitter shift register are empty. The bit is cleared when data is being been written to the transmitter FIFO. '0' – Otherwise
7	R	'1' – At least one parity error, framing error or break indications have been received and are inside the FIFO. The bit is cleared upon reading from the register. '0' – Otherwise.

4.1.13.2.7 Modem Status Register (MSR)

The register displays the current state of the modem control lines. Also, four bits also provide an indication in the state of one of the modem status lines. These bits are set to '1' when a change in corresponding line has been detected and they are reset when the register is being read.

Bit #	Access	Description
0	R	Delta Clear To Send (DCTS) indicator '1' – The CTS line has changed its state.
1	R	Delta Data Set Ready (DDSR) indicator '1' – The DSR line has changed its state.
2	R	Trailing Edge of Ring Indicator (TERI) detector. The RI line has changed its state from low to high state.
3	R	Delta Data Carrier Detect (DDCD) indicator '1' – The DCD line has changed its state.
4	R	Complement of the CTS input or equals to RTS in loopback mode.
5	R	Complement of the DSR input or equals to DTR in loopback mode.
6	R	Complement of the RI input or equals to Out1 in loopback mode.
7	R	Complement of the DCD input or equals to Out2 in loopback mode.

4.1.13.2.8 Divisor Latches

The divisor latches can be accessed by setting the 7th bit of LCR to '1'. You should restore this bit to '0' after setting the divisor latches in order to restore access to the other registers that occupy the same addresses. The 2 bytes form one 16-bit register, which is internally accessed as a single number. You should therefore set all 2 bytes of the register to ensure normal operation. The register is set to the default value of **0 on reset**, which disables all serial I/O operations in order to ensure explicit setup of the register in the software. The value set should be equal to (system clock speed) / (16 x desired baud rate).
The internal counter starts to work when the LSB of DL is written, so when setting the divisor, write the MSB first and the LSB last.

4.1.14 SPI-Interface

An external SPI controller is used on the Au1250 CPU to support the the serial protocol interface (SPI). The SPI-IP is integrated in the FPGA. The SPI Interface is available on the EXM32 Connector.

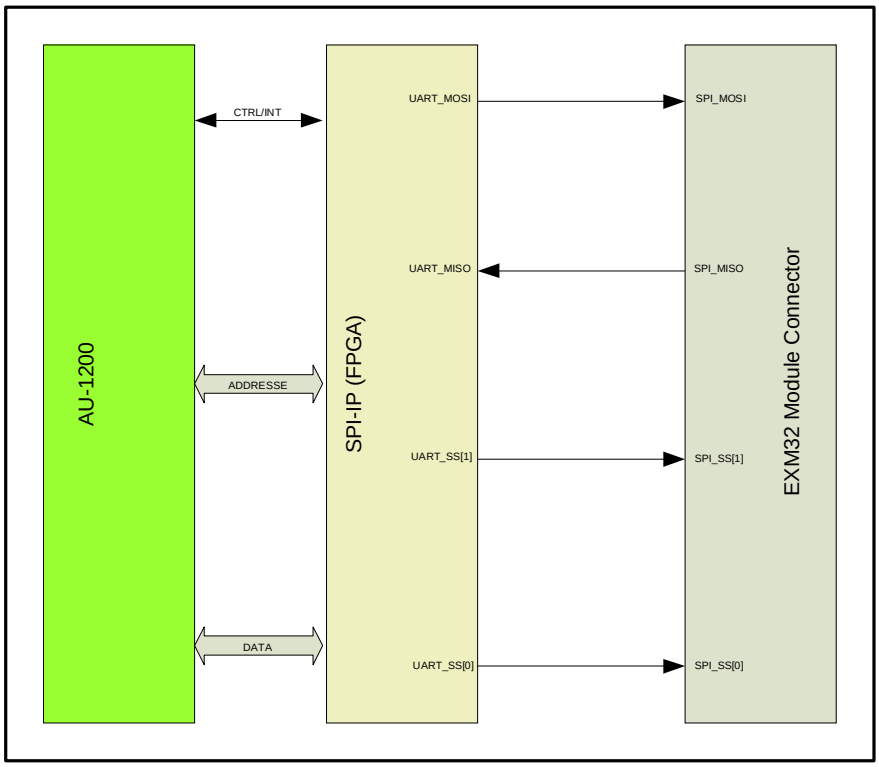


Figure 10: EXM32-Au1250 SPI interface

4.1.14.1 SPI Clock

The variable SPI Clock depends on the used CPU frequency. Refer to chapter 5.1.1 CPU for details. The clock divider register has to be initialized according to the used clock frequency.

Name	Source	Min	Max	Resolution	Description
clk	AU1250 CLKOUT	113 bps	7.373 Mbps		

4.1.14.2 SPI Core Registers

Base Address: 0x1FFF2000/ 0x3FFF2000

Name	**Address offset**	**Width**	**Access**	Description
Rx0	0x00	16	R	Data receive register 0
Rx1	0x02	16	R	Data receive register 1
Rx2	0x04	16	R	Data receive register 2
Rx3	0x06	16	R	Data receive register 3
Rx4	0x08	16	R	Data receive register 4
Rx5	0x0a	16	R	Data receive register 5
Rx6	0x0c	16	R	Data receive register 6
Rx7	0x0e	16	R	Data receive register 7
Tx0	0x00	16	R/W	Data transmit register 0
Tx1	0x02	16	R/W	Data transmit register 1
Tx2	0x04	16	R/W	Data transmit register 2
Tx3	0x06	16	R/W	Data transmit register 3
Tx4	0x08	16	R/W	Data transmit register 4
Tx5	0x0a	16	R/W	Data transmit register 5
Tx6	0x0c	16	R/W	Data transmit register 6
Tx7	0x0e	16	R/W	Data transmit register 7
CTRL	0x10	16	R/W	Control and status register
DIVIDER	0x12	16	R/W	Clock divider register
SS	0x14	16	R/W	Slave select register

All registers are 16-bit wide and accessible only with 16 bits (all wb_sel_i signals must be active).

4.1.14.2.1 Data receive registers (RxX)

Bit #	15:0
Access	R
Name	Rx

Reset Value: 0x0000

RxX

The Data Receive registers hold the value of received data of the last executed transfer. Valid bits depend on the character length field in the CTRL register (i.e. if CTRL[9:3] is set to 0x08, bit RxL[7:0]

holds the received data). If character length is less or equal to 16 bits, Rx1-Rx7 are not used, if character length is less than 32 bits, Rx2-Rx7 are not used and so on.

NOTE: The Data Received registers are read-only registers. A Write to these registers will actually modify the Transmit registers because those registers share the same FFs.

4.1.14.2.2 Data transmit register (TxX)

Bit #	15:0
Access	R/W
Name	Tx

Reset Value: 0x0000

TxX

The Data Receive registers hold the data to be transmitted in the next transfer. Valid bits depend on the character length field in the CTRL register (i.e. if CTRL[9:3] is set to 0x08, the bit Tx0[7:0] will be transmitted in next transfer). If character length is less or equal to 16 bits, Tx1-Tx7 are not used, if character len is less than 32 bits, Tx2-Tx7 are not used and so on.

4.1.14.2.3 Control and status register (CTRL)

Bit #	15:14	13	12	11	10	9	8	7	6:0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Name	Reserved	ASS	IE	LSB	Tx_NEG	Rx_NEG	GO_BSY	Reserved	CHAR_LEN

Reset Value: 0x0000

ASS
If this bit is set, ss_pad_o signals are generated automatically. This means that slave select signal, which is selected in SS register is asserted by the SPI controller, when transfer is started by setting CTRL[GO_BSY] and is de-asserted after transfer is finished. If this bit is cleared, slave select signals are asserted and de-aserted by writing and clearing bits in SS register.

IE
If this bit is set, the interrupt output is set active after a transfer is finished. The Interrupt signal is deasserted after a Read or Write to any register.

LSB
If this bit is set, the LSB is sent first on the line (bit TxL[0]), and the first bit received from the line will be put in the LSB position in the Rx register (bit RxL[0]). If this bit is cleared, the MSB is transmitted/received first (which bit in TxX/RxX register that is depends on the CHAR_LEN field in the CTRL register).

Tx_NEG
If this bit is set, the mosi_pad_o signal is changed on the falling edge of a sclk_pad_o clock signal, or otherwise the mosi_pad_o signal is changed on the rising edge of sclk_pad_o.

Rx_NEG
If this bit is set, the miso_pad_i signal is latched on the falling edge of a sclk_pad_o clock signal, or otherwise the miso_pad_i signal is latched on the rising edge of sclk_pad_o.

GO_BSY

Writing 1 to this bit starts the transfer. This bit remains set during the transfer and is automatically cleared after the transfer finished. Writing 0 to this bit has no effect.

NOTE: All registers, including the CTRL register, should be set before writing 1 to the GO_BSY bit in the CTRL register. The configuration in the CTRL register must be changed with the GO_BSY bit cleared, i.e. two Writes to the CTRL register must be executed when changing the configuration and performing the next transfer, firstly with the GO_BSY bit cleared and secondly with GO_BSY bit set to start the transfer.
When a transfer is in progress, writing to any register of the SPI Master core has no effect.

CHAR_LEN
This field specifies how many bits are transmitted in one transfer. Up to 127 bits can be transmitted.
CHAR_LEN = 0x01 … 1 bit
CHAR_LEN = 0x02 … 2 bits
…
CHAR_LEN = 0x7f … 127 bits

4.1.14.2.4 Divider register (DIVIDER)

Bit #	15:0
Access	R/W
Name	DIVIDER

Reset Value: 0xffff

DIVIDER

The value in this field is the frequency divider of the system clock wb_clk_i to generate the serial clock on the output sclk_pad_o. The desired frequency is obtained according to the following equation:

$$f_{sclk} = \frac{f_{wb\_clk}}{(DIVIDER+1)*2}$$

4.1.14.2.5 Slave select register (SS)

Bit #	15:8	7:0
Access	R	R/W
Name	Reserved	SS

Reset Value: 0x0000

SS
If CTRL[ASS] bit is cleared, writing 1 to any bit location of this field sets the proper ss_pad_o line to an active state and writing 0 sets the line back to inactive state. If CTRL[ASS] bit is set, writing 1 to any bit location of this field will select appropriate ss_pad_o line to be automatically driven to active state for the duration of the transfer, and will be driven to inactive state for the rest of the time.

4.1.15 I²C-Interface

The EXM32-Au1250 CPU Module offers three different I²C-Bus channels. The PSC0 port of the Au1250 is configured to act as a integrated I2C-controller. The PSC0 is connected to the peripheral devices on the CPU module (EPROM, RTC, PLL) and the external I2C0 bus, available on the EXM32 Connector. Refer to the Au1250 datasheet for details. In addition two separate exernal I2C controller are available on the Au1250 CPU module. The additional external I2C Controller IPs are integrated in the FPGA.

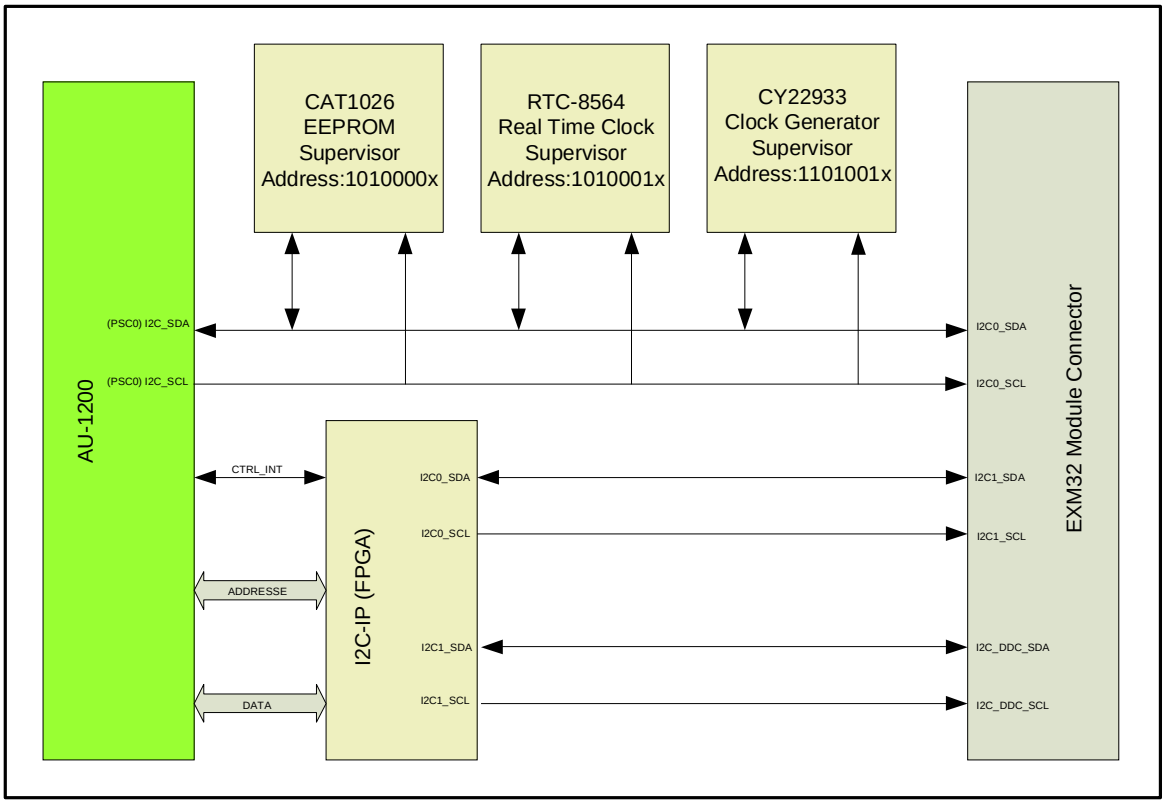


Figure 11: EXM32-Au1250 CPU-module I²C interfaces

In the following explanations only the the external I2C-controller (I2C1- and VGA_DDC_I2C-Bus) is described. For a detailed description of internal Au1250 (SMBus/-) I2C-Controller refer to the Au1250 datasheet.

4.1.15.1 Features

- Compatible with Philips I^2C standard
- Multi Master Operation
- Software programmable clock frequency
- Clock Stretching and Wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancelation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 and 10bit addressing mode
- Operates from a wide range of input clock frequencies

4.1.15.2 I²C-Clock

The external I2C-Controller clock source is the variable CPU output clock . This clock signal is feed into the SPI-controller as well. For each I2C controller a maximum wire speed of 400khz is possible.

CHANNEL	SPEED	Device	DEVICE ADDRESS
0	400 kHz/ 100kHz	Au1250 PSC interface(SMBUS)	Refer to Au12500 datasheet
1	400Khz/ 100 kHz	External I2C-Controller	0x1FFF1000/ 0x3FFF1000
DDC	400Khz/ 100 kHz	External I2C-Controller	0x1FFF1800/ 0x3FFF1800

Each I²C-Bus channel is available on the module connector/motherboard.

4.1.15.3 Registers list

Name	Address	Width	Access	Description
PRERlo	0x00	8	RW	Clock Prescale register lo-byte
PRERhi	0x01	8	RW	Clock Prescale register hi-byte
CTR	0x02	8	RW	Control register
TXR	0x03	8	W	Transmit register
RXR	0x03	8	R	Receive register
CR	0x04	8	W	Command register
SR	0x04	8	R	Status register

4.1.15.4 Register description

4.1.15.4.1 Prescale Register (PRERx)

This register is used to prescale the SCL clock line. Due to the structure of the I^2C interface, the core uses a 5*SCL clock internally. The prescale register must be programmed to this 5*SCL frequency (minus 1). Change the value of the prescale register only when the 'EN' bit is cleared.

Example1: I2C-Clock = 66 MHz, desired SCL = 100KHz

$$prescale = \frac{66\ MHz}{5 * 100\ KHz} - 1 = 131\ (dec) = 83\ (hex)$$

➔ effective SCL = 100 kHz

Example2: I2C-Clock = 66 MHz, desired SCL = 400KHz

$$prescale = \frac{66\ MHz}{5 * 400\ KHz} - 1 = 32\ (dec) = 20\ (hex)$$

➔ effective SCL = 400 kHz
Reset value: 0xFFFF

4.1.15.4.2 Control register (CTR)

Bit #	Access	Description
7	RW	EN, I^2C core enable bit. When set to '1', the core is enabled. When set to '0', the core is disabled.
6	RW	IEN, I^2C core interrupt enable bit. When set to '1', interrupt is enabled. When set to '0', interrupt is disabled.
5:0	RW	Reserved

Reset Value: 0x00

The core responds to new commands only when the 'EN' bit is set. Pending commands are finished. Clear the 'EN' bit only when no transfer is in progress, i.e. after a STOP command, or when the command register has the STO bit set. When halted during a transfer, the core can hang the I^2C bus.

4.1.15.4.3 Transmit register (TXR)

Bit #	Access	Description
7:1	W	Next byte to transmit via I^2C
0	W	In case of a data transfer this bit represent the data's LSB. In case of a slave address transfer this bit represents the RW bit. '1' = reading from slave '0' = writing to slave

Reset value: 0x00

4.1.15.4.4 Receive register (RXR)

Bit #	Access	Description
7:0	R	Last byte received via I^2C

Reset value: 0x00

4.1.15.4.5 Command register (CR)

Bit #	Access	Description
7	W	STA, generate (repeated) start condition
6	W	STO, generate stop condition
5	W	RD, read from slave
4	W	WR, write to slave
3	W	ACK, when a receiver, sent ACK (ACK = '0') or NACK (ACK = '1')
2:1	W	Reserved
0	W	IACK, Interrupt acknowledge. When set, clears a pending interrupt.

Reset Value: 0x00

The STA, STO, RD, WR, and IACK bits are cleared automatically. These bits are always read as zeros.

4.1.15.4.6 Status register (SR)

Bit #	Access	Description
7	R	RxACK, Received acknowledge from slave. This flag represents acknowledge from the addressed slave. '1' = No acknowledge received '0' = Acknowledge received
6	R	Busy, I^2C bus busy '1' after START signal detected '0' after STOP signal detected
5	R	AL, Arbitration lost This bit is set when the core lost arbitration. Arbitration is lost when: • a STOP signal is detected, but non requested • The master drives SDA high, but SDA is low. See *bus-arbitration* section for more information.
4:2	R	Reserved
1	R	TIP, Transfer in progress. '1' when transferring data '0' when transfer complete
0	R	IF, Interrupt Flag. This bit is set when an interrupt is pending, which will cause a processor interrupt request if the IEN bit is set. The Interrupt Flag is set when: • one byte transfer has been completed • arbitration is lost

Reset Value: 0x00

*Please note that all **reserved bits** are read as zeros. To ensure forward compatibility, they should be written as zeros.*

4.1.16 Audio Codec Interface (AC'97/I²S/LJ/RJ)

The EXM32-Au1250 CPU Module features one audio codec interface. This channel supports various serial interfaces (e.g. AC'97, I²S, Left Justified, Right Justified) and is configurable in master or slave mode. By default it is set to slave mode.The on-board FPGA is responsible for the audio signal routing. The register setting of the board controll register (brdctrl) determines the signal routing for the respective audio mode (AC97/I2S/master/slave). Refer to section 6.1.3 brdctrl board control register for details.

The audio codec channel is available on the EXM32 Connector /motherboard.

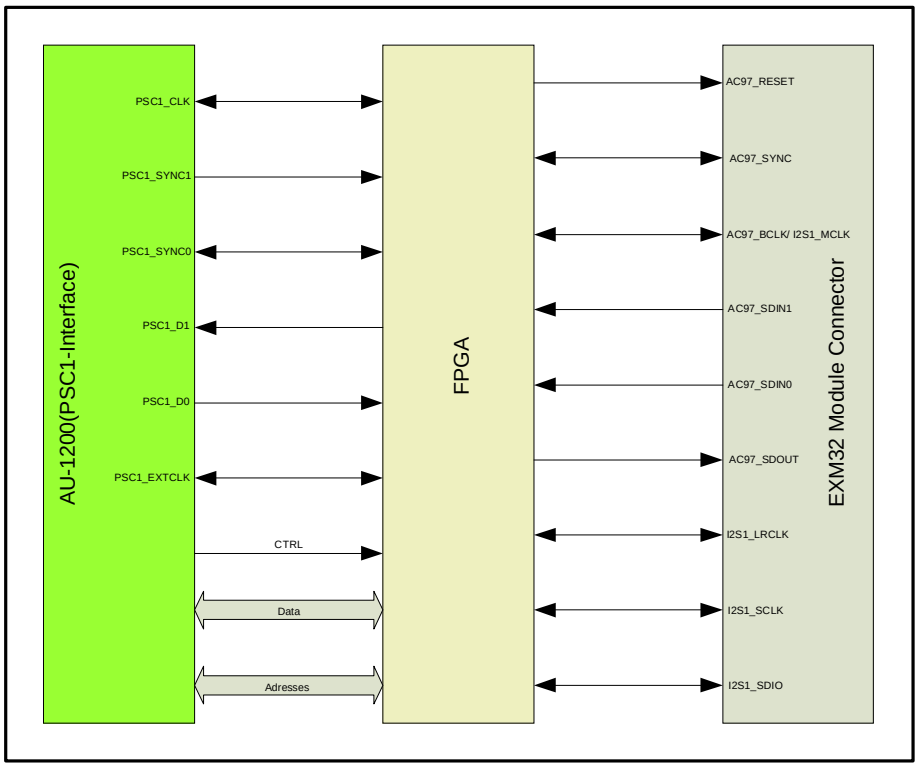


Figure 12: EXM32-Au1250 audio codec interface

Au1250 Signals	I2S		AC97	
	EXM32-Connector	Signal	EXM32-Connector	Signal
PSC1_CLK	AC97_SDIN0	SCLK	AC97_BCLK	BCLK
PSC1_SYNC1	-	-	AC_RESET	RST#
PSC1_SYNC0	AC97_SYNC	LRCLK	AC97_SYNC	SYNC
PSC1_D1	I2S1_SDIO	DIN	AC97_SDIN0	DIN
PSC1_D0	AC97_SDOUT	DOUT	AC97_SDOUT	DOUT
PSC1_EXTCLK	I2S_MCLK	MCLK	-	

4.2 Power Management

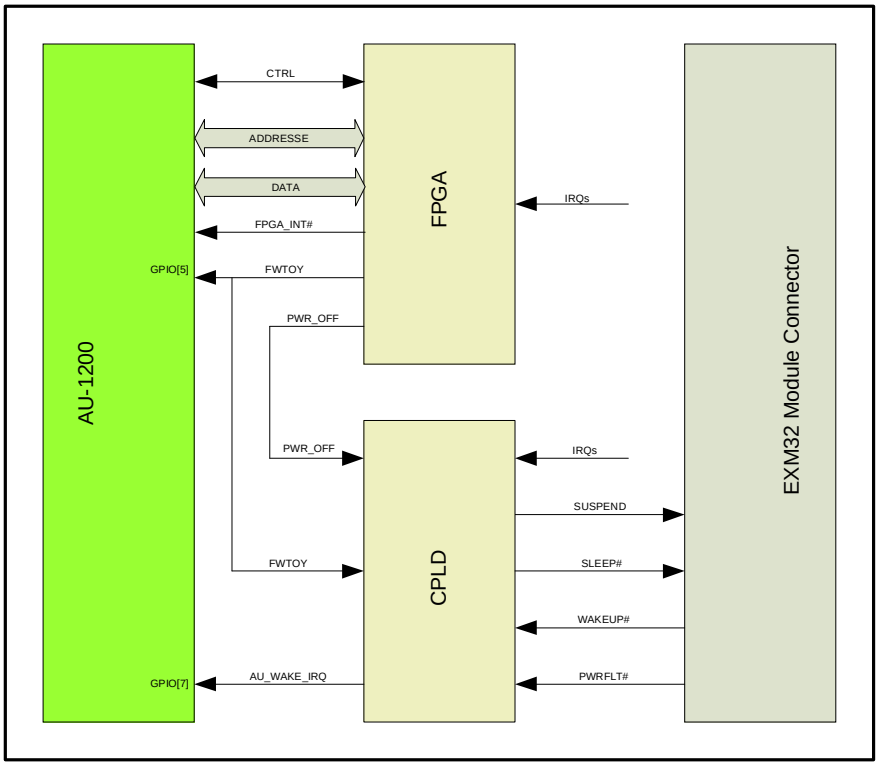


Figure 13: EXM32-Au1250 power management

The complete EXM32-System can be set to power-off, sleep or hibernate mode by the Au1250-CPU. To turn the systems power off the Au1250 has to access the Board Controll Register and set the SW_PWR_OFF bit. Refer to section 6.1.3 BRDCTRL Board Controll Register for details.
To set the EXM32-System in sleep mode follow the instructions in Au1250 datasheet section "10.4.4 Device Power Management – Sleep" for details. The System can be wake-up by asserting the wake-up interrupt signals

- AU_RTC-IRQ#
- FPGA_INT#
- AU_WAKE_IRQ#.

Refer to section 7.3 Interrupt handling of this manual and the AU1250 datasheet for details. Only the core voltage of the AU1250 is turned off in sleep mode.

To enter hibernate mode, the FWTOY bit in the board controll register of the FPGA has to be set. The FPGA releases the FWTOY signal, connected to the according pin on the AU1250 and the CPLD. The CPLD sets the SLEEP# signal. This signal is available on the EXM32-connector and can be used to shutdown external voltage regulators in the EXM32-System. A standby voltage still remains to supply the system with the required standby voltage. To enter a proper hybernate mode refer to the AU1250 datasheet for details. The EXM32-system can be wake-up by releasing the WAKEUP# signal, available on the EXM32 connector.

4.3 Data Bus

The EXM32-AU1250 is available in a standard 16-bit and in a optional 32-bit Databus version.

4.3.1 16-Bit (standard)

In the 16-bit version the 16-bit Databus of the Au1250 is buffered with a 74LVCR162245. The FPGA generates the output enable and data direction signals for the 16 bit-data buffer from the Au1250 bus state controller signals.

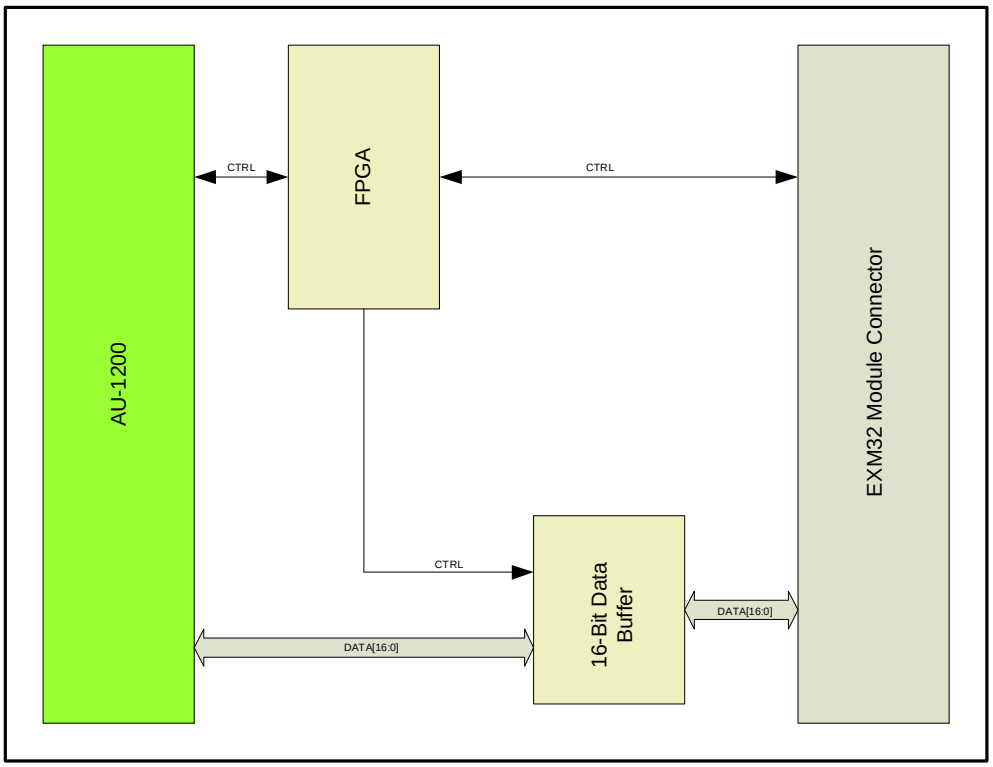
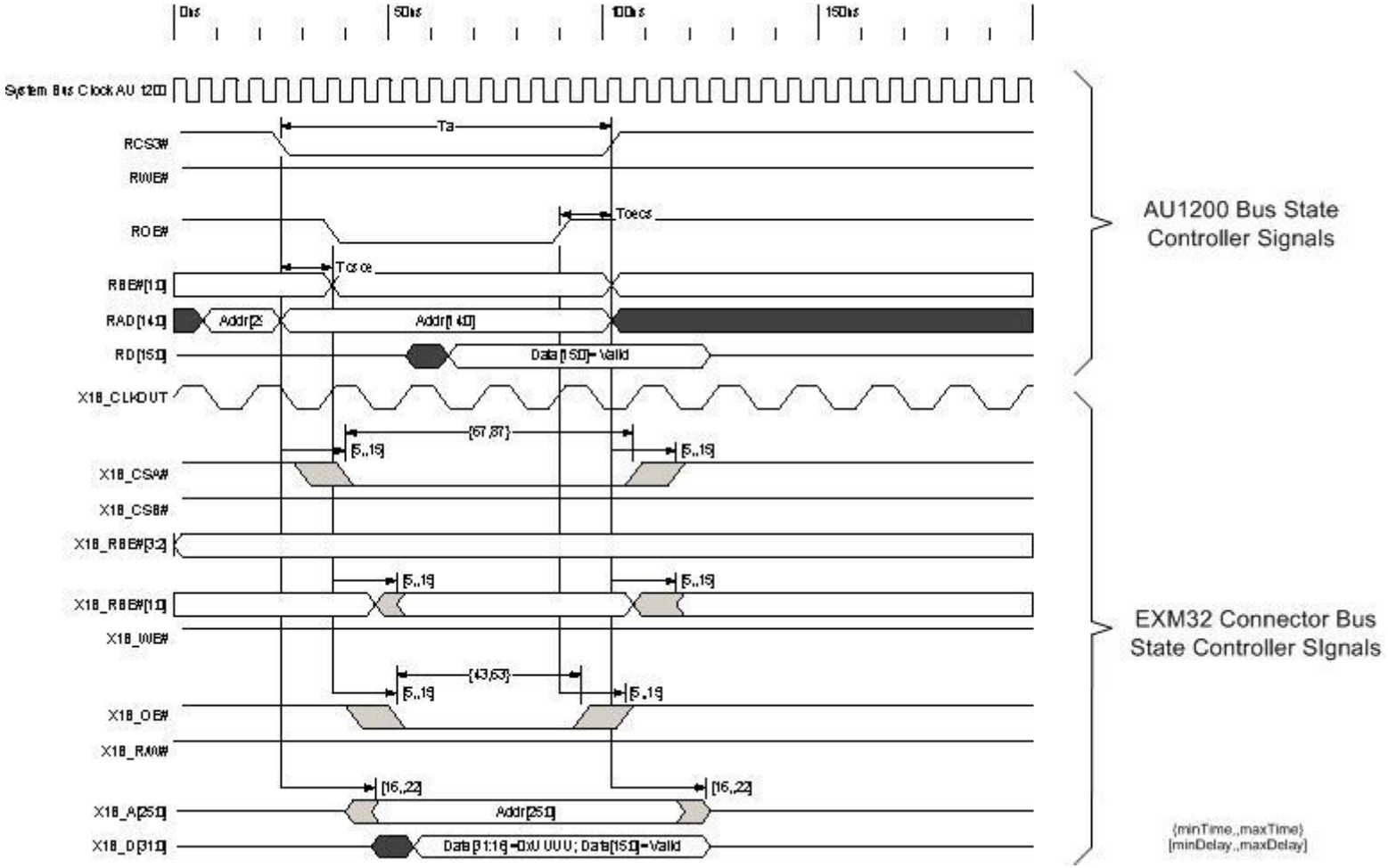


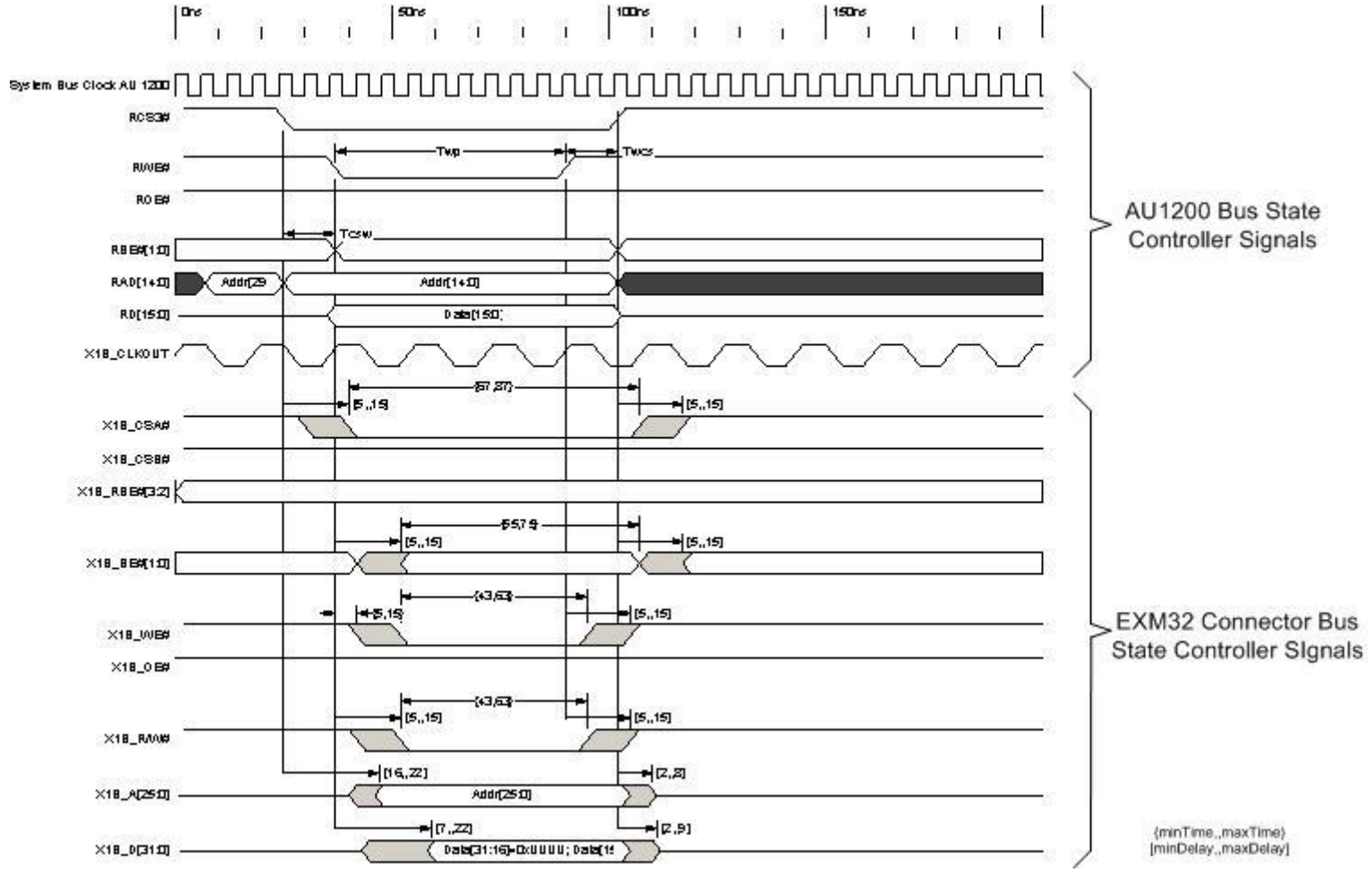
Figure 14: EXM32-Au1250 16-Bit Bus

The following timing diagrams show the EXM32-connector signals, depending on the AU1250 bus state controller signals. Refer to section 3.2 Static Bus Controller of the AU1250datasheet and section 7.4.2 Bus state controller of the EXM32-AU1250 user manual. A external 16- Bit device is connected to the bits [15:0] of the external data bus X1B_D [15:0]. The device is selected with the chip select X1B_CSA# and a address match on the Address bus X1B_A[25:1]. For the timing Values of the AU1250 Bus state controller signals Ta,Tcsoe,Tcsoe,Twp, Twcs, Tcsw refer to the AU1250 datasheet and section "Initialization". The resulting Timing Values on the EXM32 connector are affected by the delay time of the FPGA and the external bus buffers. The timing diagrams show a minimum and a maximum delay time between AU1250 bus state controller and EXM32 connector signals and the resulting minimum and maximum time for the EXM32 connector bus state controller signals. A 16 Bit device can be accessed 8 or 16 bit wide, by analysing the byte enables X1B_BE#[1:0].

4.3.1.1 16-bit read timing



4.3.2 16-write timing



4.3.3 32-Bit (optional)

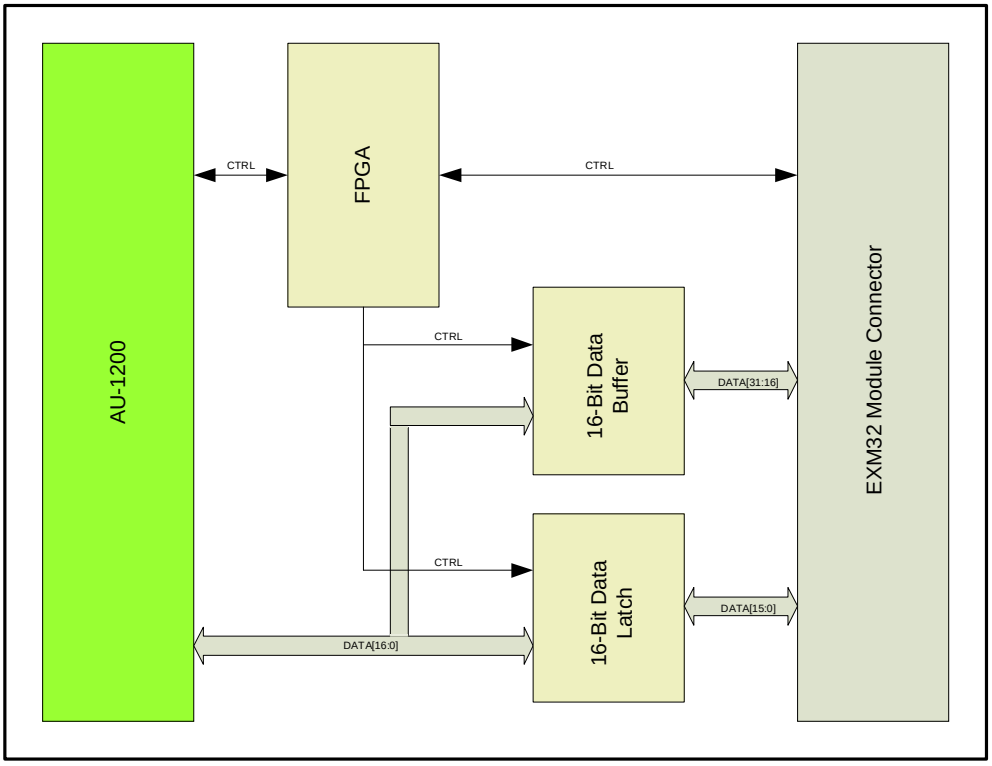
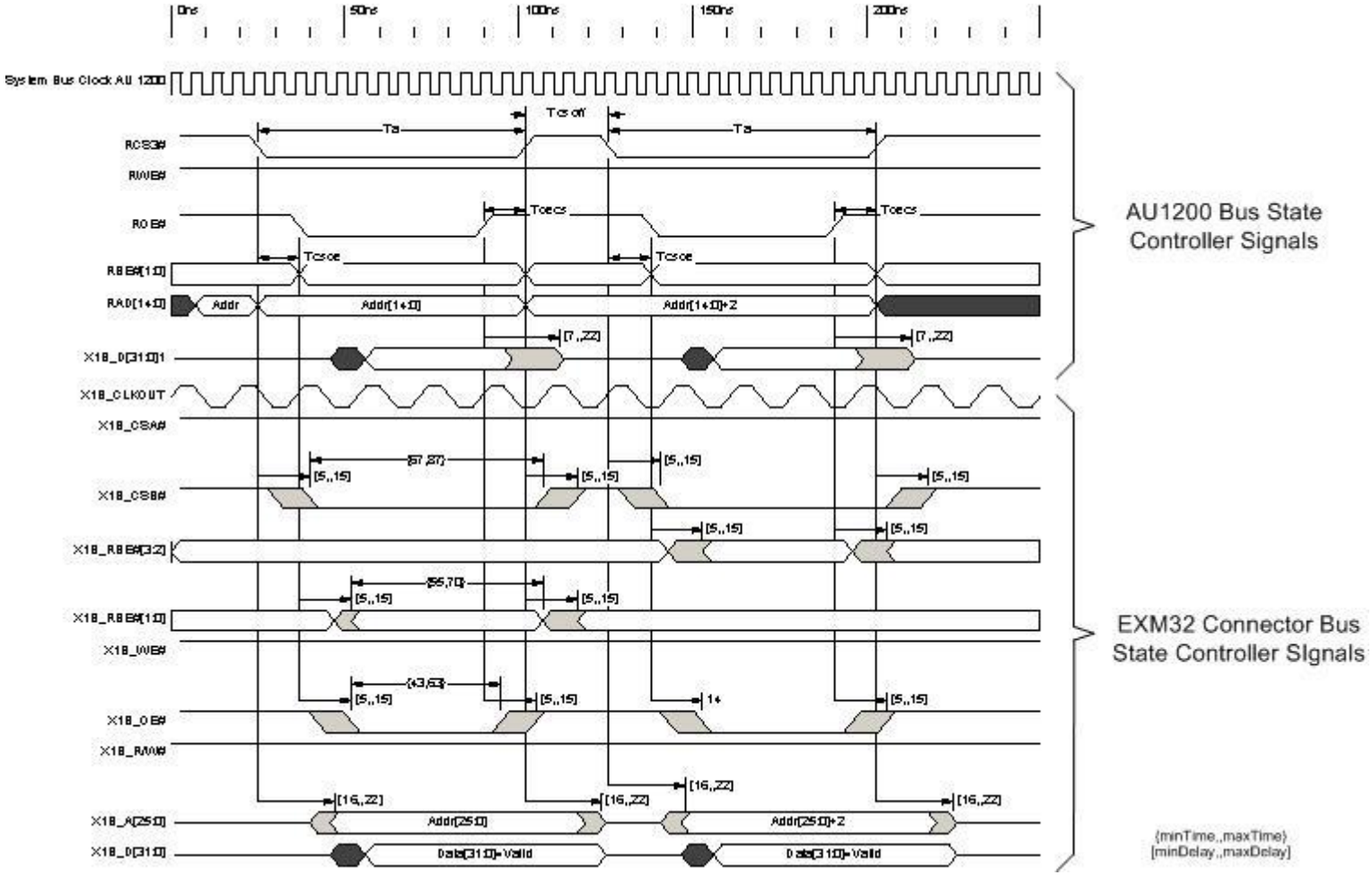


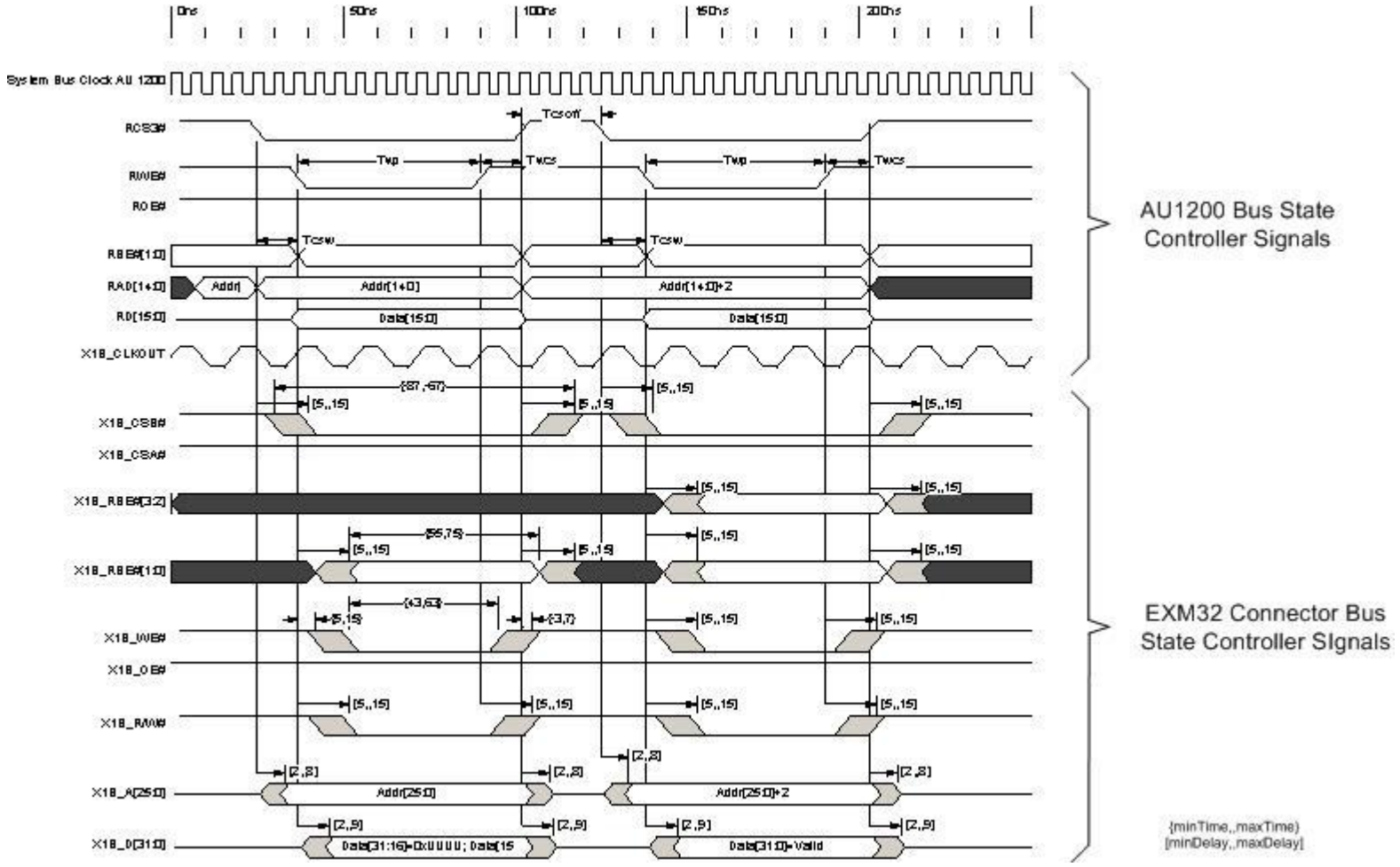
Figure 14: EXM32-Au1250 32-Bit Bus

The AU1250 CPU Module is available with an optional 32-bit data bus X1B_D[31:0]. In the 32-bit version two consecutive 16 bit accesses are necessary. With the first 16-bit access the lower 16 bit are stored in a data latch. With the second beat the upper 16 bit of the 32 bit word are issued by the AU1250. During the second beat the complete 32 bit word is available on X1B_D[31:0]. The control signals for the data latch, the data buffer and the EXM32 bus state controller are issued by the FPGA. A 32 bit databus thus isn't an advantage in access time. The time remains the same like in two separate 16 bit memory accesses. A 32 bit device is always selected with the chip select X1B_CSB# and an address match on the address bus X1B_A[25:2]. A 8, 16 and 32 bit access is possible on a 32 bit device by analyzing the byte enable X1B_BE[3:0]. The AU1250 timing values in the timing diagrams Ta, Toecs, Tcoes, Twcs, Tcsw and Tcsoff are defined by initialization. The values on the EXM32 connector show the minimum and maximum possible timing for this signals. The timing diagrams show the minimum timing requirements for a 32 bit read/write access. To guarantee the correct function of the AU1250 CPU module it is prohibited to change this values. To extend access time the signal X1B_RDY, available on the EXM32 connector, has to be pulled low. The cycle is extended until the signal is released. The chip select X1B_CSA# and X1B_CSB# are configured in normal mode, no page mode is possible.

4.3.3.1 32-bit read timing



4.3.3.2 32-bit read timing



4.4 Power Supply

EXM32 Modules are supplied via the EXM32 Elastomeric Connectors X1 and X2 form the EXM32 Motherboards power supplies.

The maximum available current is:

- Main supply voltage: 3.3 VDC ±5%
  current rating: max. 8.8 A
- Optional supply voltage: 5.0 VDC ±10%
  current rating: max. 2,0 A
- Battery supply voltage: 2.4 .. 3.6 VDC
  current rating: max. 100 mA
- Standby supply voltage (for SDRAM): 3.3 VDC ±5%
  current rating: max. 100 mA

5 FPGA

(Software Driver required)

The EXM-AU1250 module is equipped with a LFEC3E FPGA. This programmable logic device controls many operations of the CPU-Module:

- address decoding
- address- and data-buffer control
- LED control
- Hardware Power Saving Modes control
- Control for 32Bit Data Bus Mode
- Integrated SPI Master
- 2 Integrated I2C Master
- Integrated UART 16550
- LCD Power-up Controller

The FPGA I/O space is mapped into area 0 (RCE3) and area 3 (RCE3). The FPGA shares its I/O space with the Ethernet Controller, CAN Controller and external chip select CSA and CSB memory space.

Example (preliminary):

IRQ	BIT	SIGNAL	DESCRIPTION	INTEVT CODE
IRQ15	15	PWRFLT#	Primary Power Supply Fault	
IRQ14	14	I2C1_IRQ	I2C1 controller interrupt	
IRQ13	13	I2CDDC_IRQ	I2CDDC controller interrupt	
IRQ12	12	SPI_IRQ	SPI controller interrupt	
IRQ11	11	CF0_IRQ	CF/ATA0 interrupt	
IRQ10	10	CF1_IRQ	CF/ATA1 interrupt	
IRQ9	9	CF0_CD	CF0 card detect	
IRQ8	8	CF1_CD	CF1 card detect	
IRQ7	7	SDIO_CD	SD card detect	
IRQ6	6	UART0_IRQ	UART0 interrupt	
IRQ5	5	UART1_IRQ	UART1 interrupt	
IRQ4	4	UART2_IRQ	UART2 interrupt	
IRQ3	3	CAN0_IRQ	reserved for CAN0 interrupt	
IRQ2	2	CAN1_IRQ	reserved for CAN1 interrupt	
IRQ1	1	CAN0_ERR	CAN channel 0 error interrupt	
IRQ0	0	CAN1_ERR	CAN channel 1 error interrupt	

5.1 FPGA Register Description

REGISTER	ACCESS	SIZE	RCE0 ADDRESS	RCE3 ADDRESS	RESET VALUE	INIT VALUE
BRDREV	R	16	0x1FFF_0000	0x3FFF_0000	-	
BRDSTAT	R	16	0x1FFF_0004	0x3FFF_0004	-	
BRDCTRL	R/W	16	0x1FFF_0008	0x3FFF_0008	0x0000	
LEDCTRL	R/W	16	0x1FFF_000C	0x3FFF_000C	0x0000	
LCDCTRL	R/W	16	0x1FFF_0010	0x3FFF_0010	0x0000	
CFCTRL	R/W	16	0x1FFF_0014	0x3FFF_0014	0x0000	
PDCTRL	R/W	16	0x1FFF_0018	0x3FFF_0018	0x0000	
FWCTRL	R/W	16	0x1FFF_001C	0x3FFF_001C	0x0000	
IRQCLREN	R/W	16	0x1FFF_0020	0x3FFF_0020	0x0000	
IRQSETEN	R/W	16	0x1FFF_0024	0x3FFF_0024	0x0000	
IRQCLRMSK	R/W	16	0x1FFF_0028	0x3FFF_0028	0x0000	
IRQSETMSK	R/W	16	0x1FFF_002C	0x3FFF_002C	0x0000	
SIGSTAT	R	16	0x1FFF_0030	0x3FFF_0030	-	
IRQSTAT	R	16	0x1FFF_0034	0x3FFF_0034	0x0000	
SWITCHES	R	16	0x1FFF_0038	0x3FFF_0038	-	
GPOUT	R/W	16	0x1FFF_003C	0x3FFF_003C	0x0000	
GPIO_DIR	R/W	16	0x1FFF_0040	0x3FFF_0040	0x00FF	
GPIO_DOUT	R/W	16	0x1FFF_0044	0x3FFF_0044	0x0000	
GPIO_PINSTAT	R	8	0x1FFF_0048	0x3FFF_0048		
TST_REG_IN0	R	16	0x1FFF_00E0	0x3FFF_00 E0		
TST_REG_IN1	R	16	0x1FFF_00E4	0x3FFF_00 E4		
TST_REG_IN2	R	16	0x1FFF_00E8	0x3FFF_00 E8		
TST_REG_IN3	R	16	0x1FFF_00EC	0x3FFF_00 EC		
TST_REG_OUT0	R/W	16	0x1FFF_00F0	0x3FFF_00F0	0x0000	
TST_REG_OUT1	R/W	16	0x1FFF_00F4	0x3FFF_00F4	0x0000	
TST_REG_OUT2	R/W	16	0x1FFF_00F8	0x3FFF_00F8	0x0000	
TST_REG_OUT3	R/W	16	0x1FFF_00FC	0x3FFF_00FC	0x0000	

5.1.1 BRDREV Board Revision Register (Offset 0x00)

entspricht WHO_AM_I

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	NAME	VALUE	DESCRIPTION
15 - 12	HW REV	-	CPU-Module Revision
11 - 8	HW SUBREV	-	CPU-Module Subrevision
7 - 4	FPGA REV	-	FPGA Software Revision, used for major updates
3 - 0	FPGA SUBREV	-	FPGA Software Subrevision, used for minor updates

5.1.2 BRDSTAT Board Status Register (Offset 0x04)

entspricht BOARD_STATUS

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	1	1/0	0	0	1/0	1/0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	USB OC	0	USB Overcurrent
		1	USB no Overcurrent
10	SDIO WP	0	SD-Card is fully accessible
		1	SD-Card is write protected
9	-	0	
		1	
8	FLASH BUSY#	0	Flash device is busy
		1	Flash device is idle
7	-	0	
		1	
6	SWAP BOOT	0	boot from ROM
		1	boot from FLASH
5 4	CPUID	00	reserved
		01	CPU Module #1
		10	CPU Module #2
		11	CPU Module #3
3 2	CF1 VS	00	3.3 V (default)
		01	3.3 V or 5.0 V
		10	3.3 V
		11	5.0 V
1 0	CF0 VS	00	3.3 V (default)
		01	3.3 V or 5.0 V
		10	3.3 V
		11	5.0 V

5.1.3 BRDCTRL Board Control Register (Offset 0x08)

entspricht SYSTEM_CONTROL und CONTROL / RESETS

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	SW RST	0	De-assert System Reset
		1	Assert System Reset
14	SW PWR OFF	0	no change
		1	turn off power supply
13	PSC1 CFG	0	AC97 selection
		1	I2S selection (default)
12	-	0	
		1	
11	-	0	
		1	
10	FWTOY	0	normal operation(Default)
		1	set system to hibernate mode
9	-	0	
		1	
8	-	0	
		1	
7			
6	Test Mode Enable	0	Test Mode is deactivated
		1	Test Mode is activated. Certain EXM Signals can be set/read manually in TST_REG_IN/OUT. (V0.6 Update)
5	LCD2 ENABLE	0	LCD2-/GPIO-Interface is configured in LCD Mode
		1	LCD2-/GPIO-Interface is configured in GPIO Mode
4	FLWE	0	Flash is write protected (common for Strata-Flash and NAND-Flash)
		1	Flash is fully accessible
3	-	0	
		1	
2	ETH RST	0	De-assert Ethernet Controller Reset
		1	Assert Ethernet Controller Reset
1	PD RST	0	De-assert Peripheral Devices Reset
		1	Assert Peripheral Devices Reset
0	MB RST	0	De-assert Motherboard Reset
		1	Assert Motherboard Reset

5.1.4 LEDCTRL LED Control Register (Offset 0x0C)

entspricht DISC_LEDS

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	-	0	
		1	
6	-	0	
		1	
5	-	0	
		1	
4	-	0	
		1	
3	LED4 IDLE	0	LED4 is turned off (green)
		1	LED4 is turned on (green)
2	LED3	0	LED3 is turned off (red)
		1	LED3 is turned on (red)
1	LED2	0	LED2 is turned off (yellow/green)
		1	LED2 is turned on (yellow/green)
0	LED1	0	LED1 is turned off (yellow)
		1	LED1 is turned on (yellow)

5.1.5 LCDCTRL LCD Control Register (Offset 0x10)

entspricht BOARD_SPECIFIC

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	LCD_CLK_SEL	0	LCD Display is feed by AU1250 (Default)
		1	LCD Display is feed by Spread Spectrum Clock Modulator
8:7	CM_CR_SEL[1:0]	Clock Range and Dither Rate Select. Three-level input that determines the dither rate	
		CM_CR_SEL[1:0	**CLKIN Range** / **Dither Rate**
		10	66MHz to 134MHz / fIN/2048
		01	33MHz to 80MHz / fIN/1024
		00 (Default)	20MHz to 38MHz / fIN/512
6	CM_ENABLE	0	Spread Spectrum Modulator disabled (Default)
		1	Spread Spectrum Modulator enabled
5:4	CM_SEL[1:0]	Spread-Spectrum Magnitude Select Inputs. These digital inputs select the desired spread-spectrum magnitude as shown in the table below	
		CM_SEL[1:0]	Magnitude
		11	±0.5%
		10	±1%
		01	±1.5%
		00(Default)	±2%
3	LCD DON	0	Display off (only STN displays)
		1	Display on (only STN displays)
2	LCD BLON	0	disable backlight
		1	enable backlight
1	LCD VDON	0	disable digital power supply (VDD)
		1	enable digital power supply (VDD)
0	LCD VCON	0	disable power inverter voltage (VEE)
		1	enable power inverter voltage (VEE)

5.1.6 CFCTRL Compact Flash Control Register (Offset 0x14)

entspricht PCMCIA_CONTROL

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	CF1 RST	0	De-assert Compact Flash Card 1 Reset
		1	Assert Compact Flash Card 1 Reset
14	-	0	
		1	
13	-	0	
		1	
12	CF1 EN	0	Disable Compact Flash 1 Interface
		1	Enable Compact Flash 1 Interface
11 10	CF1 VCC	00	power supply disabled
		01	set CF1 card power supply to 3.3 V
		10	set CF1 card power supply to 5.0 V (not supported by EXM-AU1250)
		11	set CF1 card power supply to 3.3 V
9	-	0	
		1	
8	-	0	
		1	
7	CF0 RST	0	De-assert Compact Flash Card 0 Reset
		1	Assert Compact Flash Card 0 Reset
6	-	0	
		1	
5	ATA0_ EN	0	Compact Flash Interrupt
		1	IDE Interrupt
4	CF0 EN	0	Disable Compact Flash 0 Interface
		1	Enable Compact Flash 0 Interface
3 2	CF0 VCC	00	power supply disabled
		01	set CF0 card power supply to 3.3 V
		10	set CF0 card power supply to 5.0 V (not supported by EXM-Au1250)
		11	set CF0 card power supply to 3.3 V
1	-	0	
		1	
0	-	0	
		1	

5.1.7 PDCTRL Peripheral Devices Control Register (Offset 0x18)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	CAN1 STB	0	de-assert CAN1 standby signal
		1	assert CAN1 standby signal
12	CAN1 EN	0	de-assert CAN1 enable signal
		1	assert CAN1 enable signal
11	-	0	
		1	
10	-	0	
		1	
9	CAN0 STB	0	de-assert CAN0 standby signal
		1	assert CAN0 standby signal
8	CAN0 EN	0	de-assert CAN0 enable signal
		1	assert CAN0 enable signal
7	-	0	
		1	
6	-	0	
		1	
5	USB1 TRI	0	X2A_USB1_PWEN is high impedance
		1	X2A_USB1_PWEN is has a defined value (PDCTRL[4])
4	USB1 PWEN	0	USB1 power disable
		1	USB1 power enable
3	-	0	
		1	
2	-	0	
		1	
1	-	0	
		1	
0	USB0 PWEN	0	USB0 power disable
		1	USB0 power enable

5.1.8 IRQSETEN IRQ Set Enable Register (Offset 0x20)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	IRQ15 EN	0	Power Fault Interrupt is disabled
		1	Power Fault Interrupt is enabled
14	IRQ14 EN	0	I2C1 Interrupt is disabled
		1	I2C1 Interrupt is enabled
13	IRQ13 EN	0	I2CDDC Interrupt is disabled
		1	I2CDDC Interrupt is enabled
12	IRQ12 EN	0	SPI Interrupt is disabled
		1	SPI Interrupt is enabled
11	IRQ11 EN	0	CF0/ATA0 interrupt is disabled
		1	CF0/ATA0 interrupt is enabled
10	IRQ10 EN	0	CF1/ATA1 interrupt is disabled
		1	CF1/ATA1 interrupt is enabled
9	IRQ9 EN	0	CF0 card detect interrupt is disabled
		1	CF0 card detect interrupt is enabled
8	IRQ8 EN	0	CF1 card detect interrupt is disabled
		1	CF1 card detect interrupt is enabled
7	IRQ7 EN	0	SD card detect interrupt is disabled
		1	SD card detect interrupt is enabled
6	IRQ6 EN	0	UART0 Interrupt is disabled
		1	UART0 Interrupt is enabled
5	IRQ5 EN	0	UART1 Interrupt is disabled
		1	UART1 Interrupt is enabled
4	IRQ4 EN	0	UART2 Interrupt is disabled
		1	UART2 Interrupt is enabled
3	IRQ3 EN	0	CAN0 controller interrupt is disabled
		1	CAN0 controller interrupt is enabled
2	IRQ2 EN	0	CAN1 controller interrupt is disabled
		1	CAN1 controller interrupt is enabled
1	IRQ1 EN	0	CAN0 error interrupt is disabled
		1	CAN0 error interrupt is enabled
0	IRQ0 EN	0	CAN1 error interrupt is disabled
		1	CAN1 error interrupt is enabled

5.1.9 IRQCLREN IRQ Clear Enable Register (Offset 0x24)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	IRQ15 EN	0	Power Fault Interrupt is disabled
		1	Power Fault Interrupt is enabled
14	IRQ14 EN	0	I2C1 Interrupt is disabled
		1	I2C1 Interrupt is enabled
13	IRQ13 EN	0	I2CDDC Interrupt is disabled
		1	I2CDDC Interrupt is enabled
12	IRQ12 EN	0	SPI Interrupt is disabled
		1	SPI Interrupt is enabled
11	IRQ11 EN	0	CF0/ATA0 interrupt is disabled
		1	CF0/ATA0 interrupt is enabled
10	IRQ10 EN	0	CF1/ATA1 interrupt is disabled
		1	CF1/ATA1 interrupt is enabled
9	IRQ9 EN	0	CF0 card detect interrupt is disabled
		1	CF0 card detect interrupt is enabled
8	IRQ8 EN	0	CF1 card detect interrupt is disabled
		1	CF1 card detect interrupt is enabled
7	IRQ7 EN	0	SD card detect interrupt is disabled
		1	SD card detect interrupt is enabled
6	IRQ6 EN	0	UART0 Interrupt is disabled
		1	UART0 Interrupt is enabled
5	IRQ5 EN	0	UART1 Interrupt is disabled
		1	UART1 Interrupt is enabled
4	IRQ4 EN	0	UART2 Interrupt is disabled
		1	UART2 Interrupt is enabled
3	IRQ3 EN	0	CAN0 controller interrupt is disabled
		1	CAN0 controller interrupt is enabled
2	IRQ2 EN	0	CAN1 controller interrupt is disabled
		1	CAN1 controller interrupt is enabled
1	IRQ1 EN	0	CAN0 error interrupt is disabled
		1	CAN0 error interrupt is enabled
0	IRQ0 EN	0	CAN1 error interrupt is disabled
		1	CAN1 error interrupt is enabled

5.1.10 IRQSETMSK IRQ Set Mask Register (Offset 0x28)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT	NAME	VALUE	DESCRIPTION
15	IRQ15 MASK	0	Power Fault Interrupt is disabled
		1	Power Fault Interrupt is masked
14	IRQ14 MASK	0	I2C1 Interrupt is disabled
		1	I2C1 Interrupt is masked
13	IRQ13 MASK	0	I2CDDC Interrupt is disabled
		1	I2CDDC Interrupt is masked
12	IRQ12 MASK	0	SPI Interrupt is disabled
		1	SPI Interrupt is masked
11	IRQ11 MASK	0	CF0/ATA0 interrupt is disabled
		1	CF0/ATA0 interrupt is masked
10	IRQ10 MASK	0	CF1/ATA1 interrupt is disabled
		1	CF1/ATA1 interrupt is masked
9	IRQ9 MASK	0	CF0 card detect interrupt is disabled
		1	CF0 card detect interrupt is masked
8	IRQ8 MASK	0	CF1 card detect interrupt is disabled
		1	CF1 card detect interrupt is masked
7	IRQ7 MASK	0	SD card detect interrupt is disabled
		1	SD card detect interrupt is masked
6	IRQ6 MASK	0	UART0 Interrupt is disabled
		1	UART0 Interrupt is masked
5	IRQ5 MASK	0	UART1 Interrupt is disabled
		1	UART1 Interrupt is masked
4	IRQ4 MASK	0	UART2 Interrupt is disabled
		1	UART2 Interrupt is masked
3	IRQ3 MASK	0	CAN0 controller interrupt is disabled
		1	CAN0 controller interrupt is masked
2	IRQ2 MASK	0	CAN1 controller interrupt is disabled
		1	CAN1 controller interrupt is masked
1	IRQ1 MASK	0	CAN0 error interrupt is disabled
		1	CAN0 error interrupt is masked
0	IRQ0 MASK	0	CAN1 error interrupt is disabled
		1	CAN1 error interrupt is masked

5.1.11 IRQCLRMSK IRQ Clear Mask Register (Offset 0x2C)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT	NAME	VALUE	DESCRIPTION
15	IRQ15 MASK	0	Power Fault Interrupt is disabled
		1	Power Fault Interrupt is masked
14	IRQ14 MASK	0	I2C1 Interrupt is disabled
		1	I2C1 Interrupt is masked
13	IRQ13 MASK	0	I2CDDC Interrupt is disabled
		1	I2CDDC Interrupt is masked
12	IRQ12 MASK	0	SPI Interrupt is disabled
		1	SPI Interrupt is masked
11	IRQ11 MASK	0	CF0/ATA0 interrupt is disabled
		1	CF0/ATA0 interrupt is masked
10	IRQ10 MASK	0	CF1/ATA1 interrupt is disabled
		1	CF1/ATA1 interrupt is masked
9	IRQ9 MASK	0	CF0 card detect interrupt is disabled
		1	CF0 card detect interrupt is masked
8	IRQ8 MASK	0	CF1 card detect interrupt is disabled
		1	CF1 card detect interrupt is masked
7	IRQ7 MASK	0	SD card detect interrupt is disabled
		1	SD card detect interrupt is masked
6	IRQ6 MASK	0	UART0 Interrupt is disabled
		1	UART0 Interrupt is masked
5	IRQ5 MASK	0	UART1 Interrupt is disabled
		1	UART1 Interrupt is masked
4	IRQ4 MASK	0	UART2 Interrupt is disabled
		1	UART2 Interrupt is masked
3	IRQ3 MASK	0	CAN0 controller interrupt is disabled
		1	CAN0 controller interrupt is masked
2	IRQ2 MASK	0	CAN1 controller interrupt is disabled
		1	CAN1 controller interrupt is masked
1	IRQ1 MASK	0	CAN0 error interrupt is disabled
		1	CAN0 error interrupt is masked
0	IRQ0 MASK	0	CAN1 error interrupt is disabled
		1	CAN1 error interrupt is masked

5.1.12 SIGSTAT Signal Status Register (Offset 0x30)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	SIG15 STAT	0	PWRFLT# (active low)
		1	PWRFLT# (active low)
14	SIG14 STAT	0	I2C1_IRQ# (active low)
		1	I2C1_IRQ# (active low)
13	SIG13 STAT	0	I2CDDC_IRQ# (active low)
		1	I2CDDC_IRQ# (active low)
12	SIG12 STAT	0	SPI_IRQ (active high)
		1	SPI_IRQ (active high)
11	SIG11 STAT	0	CF0_IRQ# (active low) ATA0_IRQ (active high)
		1	CF0_IRQ# (active low) ATA0_IRQ (active high)
10	SIG10 STAT	0	CF1_IRQ# (active low) ATA1_IRQ (active high)
		1	CF1_IRQ# (active low) ATA1_IRQ (active high)
9	SIG9 STAT	0	CF0_CD# (active low)
		1	CF0_CD# (active low)
8	SIG8 STAT	0	CF1_CD# (active low)
		1	CF1_CD# (active low)
7	SIG7 STAT	0	SDIO_CD# (active low)
		1	SDIO_CD# (active low)
6	SIG6 STAT	0	UART0_IRQ (active high)
		1	UART0_IRQ (active high)
5	SIG5 STAT	0	UART1_IRQ (active high)
		1	UART1_IRQ (active high)
4	SIG4 STAT	0	UART2_IRQ (active high)
		1	UART2_IRQ (active high)
3	SIG3 STAT	0	CAN0_IRQ# (active low)
		1	CAN0_IRQ# (active low)
2	SIG2 STAT	0	CAN1_IRQ# (active low)
		1	CAN1_IRQ# (active low)
1	SIG1 STAT	0	CAN0_ERR# (active low)
		1	CAN0_ERR# (active low)
0	SIG0 STAT	0	CAN1_ERR# (active low)
		1	CAN1_ERR# (active low)

5.1.13 IRQSTAT IRQ Status Register (Offset 0x34)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	IRQ15 STAT	0	no power fault interrupt
		1	pending power fault interrupt
14	IRQ14 STAT	0	no I2C1 interrupt request
		1	Pending I2C1 interrupt request
13	IRQ13 STAT	0	no I2CDDC interrupt request
		1	pending I2CDDC interrupt request
12	IRQ12 STAT	0	no SPI interrupt request
		1	pending SPI interrupt request
11	IRQ11 STAT	0	no CF0/ATA0 interrupt
		1	pending CF0/ATA0 interrupt
10	IRQ10 STAT	0	no CF1/ATA1 interrupt
		1	pending CF1/ATA1 interrupt
9	IRQ9 STAT	0	no CF0 card detect interrupt (writing a 0 has no effect)
		1	pending CF0 card detect interrupt (writing a 1 clears the interrupt status bit to 0)
8	IRQ8 STAT	0	no CF1 card detect interrupt (writing a 0 has no effect)
		1	pending CF1 card detect interrupt (writing a 1 clears the interrupt status bit to 0)
7	IRQ7 STAT	0	no SD card detect interrupt (writing a 0 has no effect)
		1	pending SD card detect interrupt (writing a 1 clears the interrupt status bit to 0)
6	IRQ6 STAT	0	no UART0 interrupt request
		1	pending UART0 interrupt request
5	IRQ5 STAT	0	no UART1 interrupt request
		1	pending UART1 interrupt request
4	IRQ4 STAT	0	no UART2 interrupt request
		1	pending UART2 interrupt request
3	IRQ3 STAT	0	no CAN0 controller interrupt request
		1	pending CAN0 controller interrupt request
2	IRQ2 STAT	0	no CAN1 controller interrupt request
		1	pending CAN1 controller interrupt request
1	IRQ1 STAT	0	no CAN0 error interrupt request
		1	pending CAN0 error interrupt request
0	IRQ0 STAT	0	no CAN1 error interrupt request
		1	pending CAN1 error interrupt request

5.1.14 SWITCHES Board Configuration Register (Offset 0x38)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	S7	0	Big Endian
		1	Little Endian
6-3	S[6:3]	The Value in this Register sets the maximum CPU Clock Frequency	
		Switches[6:3]	Frequency (Mhz)
		1011	600
		1101	492
		1110	396
		1111	336
2	S2	0	
		1	Default
1	S1	0	
		1	Default
0	S0	0	
		1	Default

5.1.15 GPOUT General Purpose Output Register (0x3C)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	GPOUT[7]	0	Default
		1	
6	GPOUT[6]	0	Default
		1	
5	GPOUT[5]	0	Default
		1	
4	GPOUT[4]	0	Default
		1	
3	GPOUT[3]	0	Default
		1	
2	GPOUT[2]	0	Default
		1	
1	GPOUT[1]	0	Default
		1	
0	GPOUT[0]	0	Default
		1	

5.1.16 GPIO Direction Register (0x40)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

BIT	NAME	VALUE	DESCRIPTION
15	GPIO_DIR_EN [7]	0	GPIO_DIR[7] write operation is disabled
		1	GPIO_DIR[7] write operation is enabled
14	GPIO_DIR_EN [6]	0	GPIO_DIR[6] write operation is disabled
		1	GPIO_DIR[6] write operation is enabled
13	GPIO_DIR_EN [5]	0	GPIO_DIR[5] write operation is disabled
		1	GPIO_DIR[5] write operation is enabled
12	GPIO_DIR_EN [4]	0	GPIO_DIR[4] write operation is disabled
		1	GPIO_DIR[4] write operation is enabled
11	GPIO_DIR_EN [3]	0	GPIO_DIR[3] write operation is disabled
		1	GPIO_DIR[3] write operation is enabled
10	GPIO_DIR_EN [2]	0	GPIO_DIR[2] write operation is disabled
		1	GPIO_DIR[2] write operation is enabled
9	GPIO_DIR_EN [1]	0	GPIO_DIR[1] write operation is disabled
		1	GPIO_DIR[1] write operation is enabled
8	GPIO_DIR_EN [0]	0	GPIO_DIR[0] write operation is disabled
		1	GPIO_DIR[0] write operation is enabled
7	GPIO_DIR [7]	0	GPOUT[7] used as input
		1	GPOUT[7] used as output
6	GPIO_DIR [6]	0	GPOUT[6] used as input
		1	GPOUT[6] used as output
5	GPIO_DIR [5]	0	GPOUT[5] used as input
		1	GPOUT[5] used as output
4	GPIO_DIR [[4]	0	GPOUT[4] used as input
		1	GPOUT[4] used as output
3	GPIO_DIR [3]	0	GPOUT[3] used as input
		1	GPOUT[3] used as output
2	GPIO_DIR [2]	0	GPOUT[2] used as input
		1	GPOUT[2] used as output
1	GPIO_DIR [1]	0	GPOUT[1] used as input
		1	GPOUT[1] used as output
0	GPIO_DIR [0]	0	GPOUT[0] used as input
		1	GPOUT[0] used as output

5.1.17 GPIO Data Output Register (0x44)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

BIT	NAME	VALUE	DESCRIPTION
15	GPIO_DOUT_EN [7]	0	GPIO_DOUT [7] write operation is disabled
		1	GPIO_ DOUT [7] write operation is enabled
14	GPIO_DOUT_EN [6]	0	GPIO_DOUT [6] write operation is disabled
		1	GPIO_ DOUT [6] write operation is enabled
13	GPIO_DOUT_EN [5]	0	GPIO_ DOUT [5] write operation is disabled
		1	GPIO_ DOUT [5] write operation is enabled
12	GPIO_DOUT_EN [4]	0	GPIO_ DOUT [4] write operation is disabled
		1	GPIO_ DOUT [4] write operation is enabled
11	GPIO_DOUT_EN [3]	0	GPIO_ DOUT [3] write operation is disabled
		1	GPIO_ DOUT [3] write operation is enabled
10	GPIO_DOUT_EN [2]	0	GPIO_ DOUT [2] write operation is disabled
		1	GPIO_ DOUT [2] write operation is enabled
9	GPIO_DOUT_EN [1]	0	GPIO_ DOUT [1] write operation is disabled
		1	GPIO_ DOUT [1] write operation is enabled
8	GPIO_DOUT_EN [0]	0	GPIO_ DOUT [0] write operation is disabled
		1	GPIO_ DOUT [0] write operation is enabled
7	GPIO_DOUT[7]	0	
		1	
6	GPIO_DOUT [6]	0	
		1	
5	GPIO_DOUT [5]	0	
		1	
4	GPIO_DOUT [[4]	0	
		1	
3	GPIO_DOUT [3]	0	
		1	
2	GPIO_DOUT [2]	0	
		1	
1	GPIO_DOUT [1]	0	
		1	
0	GPIO_DOUT [0]	0	
		1	

5.1.18 GPIO Pin Status Register (0x48)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	GPIO_PIN_STAT[7]	0	
		1	
6	GPIO_PIN_STAT [6]	0	
		1	
5	GPIO_PIN_STAT [5]	0	
		1	
4	GPIO_PIN_STAT [4]	0	
		1	
3	GPIO_PIN_STAT [3]	0	
		1	
2	GPIO_PIN_STAT [2]	0	
		1	
1	GPIO_PIN_STAT [1]	0	
		1	
0	GPIO_PIN_STAT [0]	0	
		1	

5.1.19 Test Register 0 Input Signals (0xE0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	NAME	VALUE	DESCRIPTION
15	X2D_SDIO_CD#	0	
		1	
14	X2D_SDIO_WP	0	
		1	
13	X1D_DREQ0#	0	
		1	
12	X1D_DREQ1#	0	
		1	
11	X2D_COM1_RXD	0	
		1	
10	X2D_COM1_CTS#	0	
		1	
9	X2A_CAN1_ERR#	0	
		1	
8	X2A_USB_OC#	0	
		1	
7	X2A_CAN0_ERR#	0	
		1	
6	X1A_CF0_CD#	0	
		1	
5	X1A_CF1_CD#	0	
		1	
4	X2A_FW_LINKON	0	
		1	
3	X1C_AC97_BCLK	0	
		1	
2	X1C_AC97_SDIN1	0	
		1	
1	X1A_CF0_RDY_IRQ#	0	
		1	
0	X1A_CF1_RDY_IRQ#	0	
		1	

5.1.20 Test Register 1 Input Signals (0xE4)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	NAME	VALUE	DESCRIPTION
15	FREQUENCY_SET[1]	0	
		1	
14	FREQUENCY_SET[0]	0	
		1	
13	AU_PSC1_D0	0	
		1	
12	AU_PSC1_SYNC1	0	
		1	
11	X2D_FR_RXD	0	
		1	
10	X2D_FR_STB#	0	
		1	
9	X2D_FR_ERR#	0	
		1	
8	X1C_PWRFLT#	0	
		1	
7	X1A_SPI_MISO	0	
		1	
6	AU_PSC1_CLK	0	
		1	
5	AU_PSC1_SYNC0	0	
		1	
4	X1C_AC97_SYNC	0	
		1	
3	X2C_I2C1_SDA	0	
		1	
2	X2C_I2C1_SCL	0	
		1	
1	X2C_DDC_SCL	0	
		1	
0	X2C_DDC_SDA	0	
		1	

5.1.21 Test Register 2 Input Signals (0xE8)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	-	0	
		1	
6	-	0	
		1	
5	-	0	
		1	
4	-	0	
		1	
3	-	0	
		1	
2	X1C_AC97_SDIN0	0	
		1	
1	X1C_I2S1_SCLK	0	
		1	
0	X1C_I2S1_LRCLK	0	
		1	

5.1.22 Test Register 3 Input Signals (0xEC)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	-	0	
		1	
6	-	0	
		1	
5	-	0	
		1	
4	-	0	
		1	
3	-	0	
		1	
2	X1B_RDY	0	
		1	
1	-	0	
		1	
0	-	0	
		1	

5.1.23 Test Register 0 Output Signals (0xF0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	X2A_CAN0_EN	0	
		1	
14	X2A_FW_LPS	0	
		1	
13	X1A_CF1_RESET	0	
		1	
12	X2D_COM1_RTS#	0	
		1	
11	X2D_COM1_TXD	0	
		1	
10	X2C_LCD_DON	0	
		1	
9	X2C_LCD_VCON	0	
		1	
8	X2C_LCD_BLON	0	
		1	
7	X2C_LCD_VDON	0	
		1	
6	X1A_CF1_PWEN#	0	
		1	
5	X1A_CF0_PWEN#	0	
		1	
4	X1A_CF0_RESET	0	
		1	
3	X1A_SPI_SCK	0	
		1	
2	X1A_SPI_SS0#	0	
		1	
1	X1A_SPI_SS1#	0	
		1	
0	X1A_SPI_MOSI	0	
		1	

5.1.24 Test Register 1 Output Signals (0xF4)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	X2D_FR_EN	0	
		1	
14	X2D_FR_TXEN#	0	
		1	
13	X2D_FR_RXEN#	0	
		1	
12	X1C_AC97_RESET#	0	
		1	
11	AU_DREQ0#	0	
		1	
10	AU_DREQ1#	0	
		1	
9	AU_PSC1_D1	0	
		1	
8	AU_PSC1_EXTCLK	0	
		1	
7	X1C_AC97_RESET#	0	
		1	
6	X2A_USB1_PWEN	0	
		1	
5	X2A_USB0_PWEN	0	
		1	
4	X2A_USB1_PWEN	0	
		1	
3	XA_CAN1_EN#	0	
		1	
2	X2A_CAN0_STB#	0	
		1	
1	X1D_DACK0#	0	
		1	
0	X1D_DACK1#	0	
		1	

5.1.25 Test Register 2 Output Signals (0xF8)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	-	0	
		1	
8	-	0	
		1	
7	-	0	
		1	
6	-	0	
		1	
5	-	0	
		1	
4	-	0	
		1	
3	X2D_LCD2_EN	0	
		1	
2	X1C_AC97_SDOUT	0	
		1	
1	X2D_FR_TXD	0	
		1	
0	X2D_FR_BGE	0	
		1	

5.1.26 Test Register 3 Output Signals (0xFC)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE	DESCRIPTION
15	-	0	
		1	
14	-	0	
		1	
13	-	0	
		1	
12	-	0	
		1	
11	-	0	
		1	
10	-	0	
		1	
9	X1A_CF_CE1#	0	
		1	
8	X1A_CF_CE2#	0	
		1	
7	X1A_CF_SCKSEL	0	
		1	
6	X1B_CSB#	0	
		1	
5	X1B_BE0#	0	
		1	
4	X1B_BE1#	0	
		1	
3	X1B_BE2#	0	
		1	
2	X1B_BE3#	0	
		1	
1	X1B_BS	0	
		1	
0	X1B_R/W#	0	
		1	

6 Programming Guide

6.1 Peripheral Memory Map

For a description of the peripheral memory space please refer to the *AU1250 Hardware Manual*.

6.2 Off-chip Memory Map

The Au1250 processor supports four external chip select spaces:

AREA/ CS	OFF-CHIP Base ADDRESSES			SIZE	WAIT STATES	BUS WIDTH	INTERFACE
0	0x0_1800_0000	to	0x0_1FFF_FFFF	128MB		16-Bit	NOR Flash (BOOT)/ Peripheral Devices
1	0x0_2000_0000	to	0x0_2FFF_FFFF	256MB		16-Bit	NAND Flash
3	0x0_3000_0000	to	0x0_3FFF_FFFF	256MB		16/32-Bit	Peripheral devices
2	0xF_0000_0000	to	0xF_FFFF_FFFF	-		8/16-Bit	PCMCIA/CF

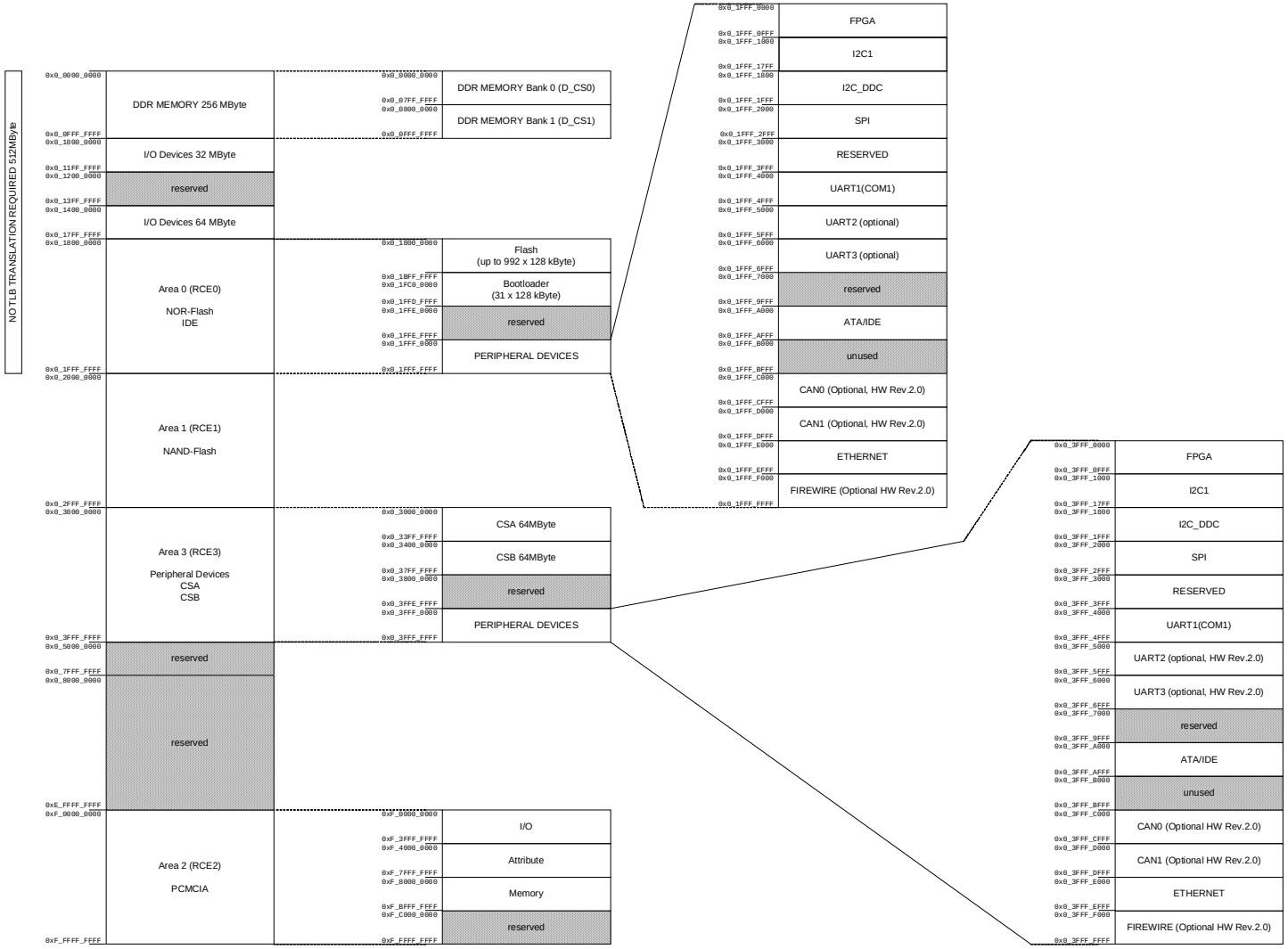


Figure 13: EXM32-Au1250 CPU-module memory map

6.2.1 DDR2 Memory Area

AU_DDR_CS0#	0x0_0000_0000
AU_DDR_CS1#	0x0_0800_0000

6.2.2 Area 0

Area 0 contains the flash memory space and I/O spaces of the peripheral devices. The whole address decoding is done by a programmable logic device (FPGA). The FPGA generates from chip select 0 multiple address decoded chip selects. One chip select for each device. The interface type of Area 0 is set to SRAM with a bus width of 16-bit.

Flash (FLASH_CS#)

FLASH base address:	0x0_1800_0000

Linear Flash memory is provided by one device. The l chip select signals for the two flash memories are address decoded. There is an Address Space of 128 MByte Reserved for Linear Flash on the Au1250 CPU Module

FPGA Register (in FPGA integrated)

FPGA base address:	0x0_1FFF_0000

I2C (in FPGA integrated)

I2C1 base address:	0x0_1FFF_1000

I2CDDC base address:	0x0_1FFF_1800

SPI (in FPGA integrated)

SPI base address:	0x0_1FFF_2000

UART16550 (in FPGA integrated)

UART0 base address:	0x0_1FFF_4000
UART1 base address (not available):	0x0_1FFF_5000
UART2 base address (not available):	0x0_1FFF_6000

ATA/IDE (ATA0_CS#, ATA1_CS#)

ATA0 base address:	0x0_1FFF_A000
ATA1 base address:	0x0_1FFF_B000

CAN (CAN0_CS#, CAN1_CS#)

CAN0 base address:	0x0_1FFF_C000

CAN1 base address:	0x0_1FFF_D000

Ethernet (ETH_CS#)

Ethernet base address:	0x0_1FFF_E000

6.2.3 Area 1

Area 1 contains the NAND Flash memory space. The Au1250 can be equipped with a optional 32 to 128 MByte NAND Flash memory device.

NAND Flash (LBSC_RCS1#)

NAND Flash base address:	0x0_2000_0000

6.2.4 Area 2

The AU1250 CPU provides the Chip Selects AU_CF_CE1#, AU_CF_CE2# instead of LBSC-RCS2. Refer to the Au1250 Datasheet for details. X1C_A26 and consequently X1A_CF_SCKSEL determines if Compact Flash or an IDE drive is selected.

X1C_A26 (X1A_CF_SCKSEL) = 0 → Compact Flash Socket A
X1C_A26 (X1A_CF_SCKSEL) = 1 → Compact Flash Socket B

Compact Flash: (AU_CF_CE1#, AU_CF_CE2#)

Compact Flash base address:	0xF_0000_0000

6.2.5 Area 3

The Area 3 Address Space is reserved for peripheral devices like SRAM or I/O devices.

CSA (X1C_CSA#))

CSA base address:	0x0_3000_0000

The CSA address space is reserved for 16-bit devices

CSB (X1C_CSB#))

CSB base address:	0x0_3400_0000

The CSB address Space is reserved for 32-bit devices

FPGA Register (in FPGA integrated)

FPGA base address:	0x0_3FFF_0000

I2C (in FPGA integrated)

I2C1 base address:	0x0_3FFF_1000

I2CDDC base address:	0x0_3FFF_1800

SPI (in FPGA integrated)

SPI base address:	0x0_3FFF_2000

UART16550 (in FPGA integrated)

UART1 (COM1) base address:	0x0_3FFF_4000
UART2 base address (not available):	0x0_3FFF_5000
UART3 base address (not available):	0x0_3FFF_6000

CAN (CAN0_CS#, CAN1_CS#)

CAN0 base address:	0x0_3FFF_C000
CAN1 base address:	0x0_3FFF_D000

Ethernet (ETH_CS#)

Ethernet base address:	0x0_3FFF_E000

6.3 Interrupt Handling

There are two types of interrupt Sources:

- Exerternal IRQ request
- Integrated Peripheral modules

The AU1250 GPIO pins are configurable as a level sensitive or edge triggered interrupt Source.

6.3.1 IRQ

There are two interrupt controllers in the Au1250 processor. Each interrupt controller supports 32 interrupt sources. Each interrupt source is individually maskable to either enable or disable the core from detecting the interrupt. Interrupts are generated by software, integrated interrupt controllers, performance counters and timers. All interrupt sources are equal in priority; that is, the interrupt sources are not prioritized in hardware. As a result, software determines the relative priority of the interrupt sources. See the Au1250 datasheet and chapter 2.6.2 Interrupt Architecture and chapter 5 Interrupt Controller for details.

Interrupt sources connected to the Au1250:

Interrupt	**Active**	**Au1250**			
		Port	**Pin**	**Interrupt Number**	**Interrupt Controller**
X1B_IRQ_EXT0#	low level	GPIO[0]	B9	0	1
X1B_IRQ_EXT1#	low level	GPIO[1]	C7	1	1
AU_RTC_IRQ#	low level	GPIO[2]	D8	2	1
FPGA_INT#	low level	GPIO[5]	C10	5	1
AU_WAKE_IRQ#	low level	GPIO[7]	A9	7	1
X1B_IRQ_MB2#	low level	GPIO[16]	C22	16	1
X1B_IRQ_MB0#	low level	GPIO[27]	D17	27	1
X1B_IRQ_MB1#	low level	GPIO[29]	C15	29	1
ETH_IRQ	high level	GPIO[31]	C21	31	1
AU_WATCHDOG	high level	GPIO[215]	D20	28	0

The FPGA Interrupt is the described in chapter 1.1.2 IRQSTAT CPLD IRQ Status Register.

The **FPGA_INT#** is the logical **or** of the signals:

Name	Description	Source
PWRFLT#	Powerfault#	EXM32-Connector
I2C0_INT#	I2C-Controller 0 Interrupt	Au1250 CPU Module
I2C1_INT#	I2C-Controller 1 Interrupt	Au1250 CPU Module
SPI_INT#	SPI_IRQ#	Au1250 CPU Module
CF0_RDY_IRQ#	Compact Flash 0 Ready Interrupt	EXM32-Connector
CF1_RDY_IRQ#	Compact Flash 1 Ready Interrupt	EXM32-Connector
CF0_CD#	Compact Flash 0 Card Detect	EXM32-Connector
CF1_CD#	Compact Flash 1 Card Detect	EXM32-Connector
SDIO_CD#	SDIO Card Detect	EXM32-Connector
UART1_INT	UART1 Interrupt	Au1250 CPU Module
UART2_INT	UART2 Interrupt (optional)	Au1250 CPU Module
UART3_INT	UART3 Interrupt (optional)	Au1250 CPU Module
CAN0_INT#	CAN-Controller 0 Interrupt	Au1250 CPU Module
CAN1_INT#	CAN-Controller 1 Interrupt	Au1250 CPU Module

CAN0_ERR#	CAN-Controller 0 Error	Au1250 CPU Module
CAN1_ERR#	CAN-Controller 1 Error	Au1250 CPU Module

To detect the wake-up interrupt source the Interrupt Status register has to be read out. Refer to section 1.1.2 IRQSTAT CPLD IRQ Status Register for details.

The **AU_WAKE_IRQ#** is the logical **or** of the signals:

Name	Description	Source
AU_PM_WAKE#	Wake up from hibernate	Au1250
WAKEUP		EXM32-Connector
IRQ_EXT1#	Extension module 1 Interrupt	EXM32-Connector
IRQ_EXT0#	Extension module 0 Interrupt	EXM32-Connector
IRQ_MB2#	Motherboard 2 Interrupt	EXM32-Connector
IRQ_MB1#	Motherboard 1 Interrupt	EXM32-Connector
IRQ_MB0#	Motherboard 0 Interrupt	EXM32-Connector
WATCHDOG	Externer Watchdogtimer Interrupt (optional)	Au1250 CPU module
ETH_IRQ	Ethernet Interrupt	Au1250 CPU module

Both Signals FPGA_INT#, AU_WAKE_IRQ# and AU_RTC_IRQ# can generate a Wake up interrupt to the Au1250 CPU.

6.4 Au1250 Initialisation (preliminary)

6.4.1 Clock

CPU PLL Control

sys_cpupll **Address: 0x0_1190_0060**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0

0x0000001C (INIT (336Mhz))
0x00000021 (INIT (396Mhz))
0x00000029 (INIT (492Mhz))
0x00000032 (INIT (600Mhz))

6.4.2 Bus State Controller

6.4.2.1 Configuration for RCS0 (SRAM/ On-board Peripherals)

Chip Select 0 Configuration Register

mem_stcfg0 **Address: 0x0_1400_1000**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1
INIT (336Mhz)	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0
INIT (396Mhz)	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0

INIT (492Mhz)	0	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0
INIT (600Mhz)	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0

0x003D40C0 (INIT (336Mhz))
0x003D40C0 (INIT (396Mhz))
0x003D60C0 (INIT (492Mhz))
0x003D40C0 (INIT (600Mhz))

Chip Select 0 Timing Register

mem_sttime0 **Address: 0x0_1400_1004**

BIT	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT (336Mhz)	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1
INIT (396Mhz)	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1
INIT (492Mhz)	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1
INIT (600Mhz)	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	1

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

0x06610002 (INIT (336Mhz))
0x06610002 (INIT (396Mhz))
0x06610002 (INIT (492Mhz))
0x06610002 (INIT (600Mhz))

Chip Select 0 Adress Region Register

mem_staddr0 **Address: 0x0_1400_1008**

BIT	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	0	0	1	1	1	1	1	1	1	0	0
INIT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

BIT	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0

0x10003000

6.4.2.2 Configuration for RCS1 (NAND-Flash)

Chip Select 1 Configuration Register

mem_stcfg1 **Address: 0x0_1400_1010**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1

0x00450045 (INIT (336Mhz))
0x00450045 (INIT (396Mhz))
0x00450045 (INIT (492Mhz))
0x00450045 (INIT (600Mhz))

Chip Select 1 Timing Register

mem_sttime1 **Address: 0x0_1400_1014**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1
INIT (336Mhz)	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0	0
INIT (396Mhz)	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0	0
INIT (492Mhz)	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0	0
INIT (600Mhz)	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0	0

0x00006664 (INIT (336Mhz))
0x00007774 (INIT (396Mhz))
0x00009996 (INIT (492Mhz))
0x00007774 (INIT (600Mhz))

Chip Select 1 Adress Region Register

mem_staddr1 **Address: 0x0_1400_1018**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0

0x12503C00

6.4.2.3 Configuration for RCS2 (Compact Flash/ PCMCIA)

Chip Select 2 Configuration Register

mem_ stcfg2 **Address: 0x0_1400_1020**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
INIT (492Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0

0x00040042 (INIT (336Mhz))
0x00040042 (INIT (396Mhz))
0x00040042 (INIT (492Mhz))
0x00040042 (INIT (600Mhz))

Chip Select 2 Timing Register

mem_sttime2 **Address: 0x0_1400_1024**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT (336Mhz)	0	0	0	1	1	1	1	1	0	0	0	1	1	0	1	0
INIT (396Mhz)	0	0	1	0	0	1	1	0	0	0	1	0	0	0	0	0
INIT (492Mhz)	0	0	1	0	1	1	1	1	0	0	1	0	1	0	0	0
INIT (600Mhz)	0	0	1	0	0	1	1	0	0	0	1	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1
INIT (336Mhz)	0	0	1	1	1	0	1	1	1	1	1	0	1	1	0	1
INIT (396Mhz)	0	1	0	0	0	1	0	0	1	1	0	1	0	0	0	0
INIT (492Mhz)	0	1	0	1	0	1	0	1	1	1	1	1	0	1	0	0
INIT (600Mhz)	0	1	0	0	0	1	0	0	1	1	0	1	0	0	0	0

0x1F1A3BED (INIT (336Mhz))
0x262044D0 (INIT (396Mhz))
0x2F2855F4 (INIT (492Mhz))
0x262044D0 (INIT (600Mhz))

Chip Select 2 Adress Region Register

mem_staddr2 **Address: 0x0_1400_1028**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0

0x18003C00

6.4.2.4 Configuration for RCS3 (External Devices)

Chip Select 3 Configuration Register

mem_stcfg3 **Address: 0x0_1400_1030**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0
INIT (336Mhz)	0	0	1	0	0	0	1	0	0	0	1	0	1	1	0	0
INIT (396Mhz)	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0
INIT (492Mhz)	0	1	0	0	0	0	1	0	0	0	1	0	1	1	0	0
INIT (600Mhz)	0	0	0	0	0	0	1	0	0	0	1	0	1	1	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	1	0	0	0	0	0	1	1	0	0	0	0	1	1
INIT (336Mhz)	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
INIT (492Mhz)	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

0x222C00C0 (INIT (336Mhz))
0x222C00C0 (INIT (396Mhz))
0x422C00C0 (INIT (492Mhz))
0x222C00C0 (INIT (600Mhz))

Chip Select 3 Timing Register

mem_sttime3 **Address: 0x0_1400_1014**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	0	0	1	1	1	1	1	1	1	0	0
INIT (336Mhz)	0	0	0	1	0	0	1	0	0	0	1	1	0	0	0	1
INIT (396Mhz)	0	0	0	1	0	0	1	0	0	0	1	1	0	0	1	0
INIT (492Mhz)	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0
	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT (336Mhz)	1	1	0	0	0	1	0	1	1	0	0	0	1	0	1	1
INIT (396Mhz)	0	0	0	0	0	1	0	1	1	1	0	0	1	1	0	1
INIT (492Mhz)	1	0	0	0	1	0	1	0	1	0	0	0	1	1	1	1
INIT (600Mhz)	0	0	0	0	0	1	0	1	1	1	0	0	1	1	0	1

0x1231C58B (INIT (336Mhz))
0x123205CD (INIT (396Mhz))
0x22428A8F (INIT (492Mhz))
0x123205CD (INIT (600Mhz))

Chip Select 3 Adress Region Register

mem_staddr3 **Address: 0x0_1400_1018**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0

0x14003C00

6.4.2.5 Global Chip Select Configuration

Addresslatch Timing Register

mem_staltime **Address: 0x0_1400_1040**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT (336Mhz)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT (396Mhz)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT (492Mhz)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT (600Mhz)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	-	-	-	-	-	-	-	1	0	0	0	1	1	1	0	0
INIT (336Mhz)	-	-	-	-	-	-	-	0	1	0	0	0	0	0	0	1
INIT (396Mhz)	-	-	-	-	-	-	-	0	1	0	0	0	0	0	0	1
INIT (492Mhz)	-	-	-	-	-	-	-	0	1	0	0	0	0	0	0	1
INIT (600Mhz)	-	-	-	-	-	-	-	0	1	0	0	0	0	0	0	1

0x00000049 (INIT (336Mhz))
0x00000049 (INIT (396Mhz))
0x00000049 (INIT (492Mhz))
0x00000049 (INIT (492Mhz))

Static Bus NAND Control Register

mem_stndctrl **Address: 0x0_1400_1100**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W
DEFAULT	-	-	-	-	-	-	-	0	0	0	0	0	-	-	-	1
INIT	-	-	-	-	-	-	-	1	0	0	0	0	0	0	0	0

0x00000100

6.4.3 DDR2 Memory Controller

Chip Select 0 Timing Register

mem_sdmode0 **Address: 0x0_1400_0800**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	-	-	-	-	-	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	-	-	-	-	-	1	1	1	-	1	1	1	1	1	1	1
INIT (336Mhz)	-	-	-	-	-	0	0	1	-	0	1	0	0	1	1	1
INIT (396Mhz)	-	-	-	-	-	0	0	1	-	0	1	0	0	1	1	1
INIT (492Mhz)	-	-	-	-	-	0	1	0	-	0	1	1	1	0	0	1
INIT (600Mhz)	-	-	-	-	-	0	0	1	-	0	1	0	0	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
DEFAULT	-	1	1	1	-	1	1	1	-	1	1	1	-	1	1	1
INIT (336Mhz)	-	0	1	0	-	0	1	0	-	0	1	0	-	1	0	0
INIT (396Mhz)	-	0	1	0	-	0	1	0	-	0	1	0	-	1	0	0
INIT (492Mhz)	-	0	1	1	-	0	1	1	-	0	1	1	-	1	0	1
INIT (600Mhz)	-	0	1	0	-	0	1	0	-	0	1	0	-	1	0	0

0x01272224 (INIT (336Mhz))
0x01272224 (INIT (396Mhz))
0x02393335 (INIT (492Mhz))
0x01272224 (INIT (600Mhz))

Chip Select 1 Timing Register

mem_sdmode1 **Address: 0x0_1400_0808**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	-	-	-	-	-	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	-	-	-	-	-	1	1	1	-	1	1	1	1	1	1	1
INIT (336Mhz)	-	-	-	-	-	0	0	1	-	0	1	0	0	1	1	1
INIT (396Mhz)	-	-	-	-	-	0	0	1	-	0	1	0	0	1	1	1
INIT (492Mhz)	-	-	-	-	-	0	1	0	-	0	1	1	1	0	0	1
INIT (600Mhz)	-	-	-	-	-	0	0	1	-	0	1	0	0	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W	-	R/W	R/W	R/W
DEFAULT	-	1	1	1	-	1	1	1	-	1	1	1	-	1	1	1
INIT (336Mhz)	-	0	1	0	-	0	1	0	-	0	1	0	-	1	0	0
INIT (396Mhz)	-	0	1	0	-	0	1	0	-	0	1	0	-	1	0	0
INIT (492Mhz)	-	0	1	1	-	0	1	1	-	0	1	1	-	1	0	1
INIT (600Mhz)	-	0	1	0	-	0	1	0	-	0	1	0	-	1	0	0

0x01272224 (INIT (336Mhz))
0x01272224 (INIT (396Mhz))
0x02393335 (INIT (492Mhz))
0x01272224 (INIT (600Mhz))

Chip Select 0 Adress Configuration and Enable

mem_sdaddr0 **Address: 0x0_1400_0820**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W		R/W	R/W	R/W	-	R/W	R/W	R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
DEFAULT	-	0	0	0	-	0	0	1	-	-	-	0	1	1	1	1
INIT	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0

0x341503E0

Chip Select 1 Adress Configuration and Enable

mem_sdaddr1 **Address: 0x0_1400_0828**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W		R/W	R/W	R/W	-	R/W	R/W	R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
DEFAULT	-	0	0	0	-	0	0	1	-	-	-	0	1	1	1	1
INIT	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0

0x341583E0

Global Configuration Register A

mem_sdconfiga **Address: 0x0_1400_0840**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	-	R/W	R/W
DEFAULT	1	-	0	0	0	1	1	1	1	1	1	1	-	-	1	1
INIT (336Mhz)	0	-	1	1	0	0	0	1	0	0	0	1	-	-	0	0
INIT (396Mhz)	0	-	1	1	0	0	0	1	0	1	0	0	-	-	0	0
INIT (492Mhz)	0	-	1	1	0	0	0	1	1	0	0	1	-	-	0	0
INIT (600Mhz)	0	-	1	1	0	0	0	1	0	1	0	0	-	-	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
INIT (336Mhz)	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0
INIT (396Mhz)	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0
INIT (492Mhz)	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1
INIT (600Mhz)	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0

0x31100520 (INIT (336Mhz))
0x3140060A (INIT (396Mhz))
0x31900781 (INIT (492Mhz))
0x3140060A (INIT (600Mhz))

Global Configuration Register B

mem_sdconfigb **Address: 0x0_1400_0848**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	-	0	0
INIT (336Mhz)	1	0	1	0	0	0	0	0	0	0	0	0	0	-	1	0
INIT (396Mhz)	1	0	1	0	0	0	0	0	0	0	0	0	0	-	1	0
INIT (492Mhz)	1	0	1	0	0	0	0	0	0	0	0	0	0	-	1	0
INIT (600Mhz)	1	0	1	0	0	0	0	0	0	0	0	0	0	-	1	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	-	0	0	0	0	0	0
INIT (336Mhz)	0	0	0	0	0	0	0	0	0	-	0	0	1	1	0	0
INIT (396Mhz)	0	0	0	0	0	0	0	0	0	-	0	0	1	1	0	0
INIT (492Mhz)	0	0	1	0	0	0	0	0	0	-	0	0	1	1	0	0
INIT (600Mhz)	0	0	0	0	0	0	0	0	0	-	0	0	1	1	0	0

0xA002000C (INIT (336Mhz))
0xA002000C (INIT (396Mhz))
0xA002000C (INIT (492Mhz))
0xA002000C (INIT (600Mhz))

6.4.4 Interrupt Controller

Setting up the GPIOs Controller as Interrupts

sys_pinfunc **Address: 0x0 1190002C**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
INIT	1	1	0	0	0	1	1	0	0	0	0	0	1	1	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	1	-	1	0	0	0	0	0	0	1	1	1	1	-	-
INIT	1	1	-	0	1	0	0	0	1	1	0	0	1	1	-	-

0xC60CCCCC

sys_trioutclr **Address: 0x0 11900100**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	-	W	W	W	W	W	W	W	W	W	W	W	-	-
DEFAULT	0	0	-	0	0	0	0	0	0	0	0	0	0	0	-	-
INIT	0	0	-	0	0	1	1	1	0	0	0	0	1	0	-	-

0x100E0708

sys_outputclr **Address: 0x0 1190010C**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x00000000

Setting GPIO Block 2 Port Direction

gpio2_dir **Address: 0x0_1170_0000**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x00000000

Enable GPIOs Block 2 as a Interrupt Source

gpio2_inten **Address: 0x0_1170_0010**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
INIT	1	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

0x00008000

Enable Block 2

gpio2_enable **Address: 0x0_1170_0014**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
INIT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	1

0x00000001

Interrupt Controller 0 Configuration Register

The Bits in the Following Registers correspond with the interrupt described in the Following Table. Refer to the Au1250 Datasheet chapter 5.1 Interrupt Controller sources

BIT	NAME	DESCRIPTION
31	MAE Done	
30	LCD Controll	
29	USB Controller	
28	GPIO[208:215]	Optional external Watchdog Timer Interrupt (GPIO215)
27	GPIO[207]	Not Used
26	GPIO[206]	Not Used
25	GPIO[205]	Not Used
24	GPIO[204]	Not Used
23	NAND Controlller	
22	GPIO[203]	Not Used
21	RTC Match 2	
20	RTC Match 1	
19	RTC Match 0	
18	RTC(tick)	
17	TOY Match 2	

16	TOY Match 1	
15	TOY Match 0	
14	TOY (tick)	
13	Camera Interface Module	
12	AES Cryptographie Engine	
11	PSC1	
10	PSC0	
9	MAE Frontend	
8	UART1	
7	GPIO[202]	Not Used
6	GPIO[201]	Not Used
5	GPIO[200]	Not Used
4	MAE Backend	
3	DDMA Controller	
2	Secure Digital Decoder	
1	Software Counter Match	
0	UART0	

ic_cfg0set **Address: 0x0_1040_0040**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x00000000

ic_cfg1set **Address: 0x0_1040_0048**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x10000000

ic_cfg2set **Address: 0x0_1040_0050**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x10000000

Interrupt Controller 0 Source Select Register

ic_srcset **Address: 0x0_1040_0058**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0xFFFFFFFF

Interrupt Assignment Register 0

ic_assignset **Address: 0x0_1040_0060**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0xFFFFFFFF

Interrupt STAT Register 0

ic_STATset **Address: 0x0_1040_0070**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x10000000

6.4.4.1 Interrupt Controller 1

Interrupt Controller 1 Configuration Register

The Signal in the Following Table corresponds with the according Bit in the following Interrupt register

BIT	NAME	DESCRIPTION
31	GPIO[31]	ETH_IRQ
30	GPIO[30]	not used
29	GPIO[29]	X1B_IRQ_MB1#
28	GPIO[28]	not used
27	GPIO[27]	X1B_IRQ_MB0#
26	GPIO[26]	not used
25	GPIO[25]	not used
24	GPIO[24]	not used
23	GPIO[23]	not used
22	GPIO[22]	not used
21	GPIO[21]	not used
20	GPIO[20]	not used
19	GPIO[19]	not used
18	GPIO[18]	not used
17	GPIO[17]	not used
16	GPIO[16]	X1B_IRQ_MB2#
15	GPIO[15]	not used
14	GPIO[14]	not used
13	GPIO[13]	not used
12	GPIO[12]	AU_DREQ1#
11	GPIO[11]	not used
10	GPIO[10]	not used
9	GPIO[9]	not used
8	GPIO[8]	not used
7	GPIO[7]	AU_WAKE_IRQ#
6	GPIO[6]	not used
5	GPIO[5]	FPGA_INT#
4	GPIO[4]	AU_DREQ0#
3	GPIO[3]	not used
2	GPIO[2]	AU_RTC_IRQ#
1	GPIO[1]	X1B_IRQ_EXT1#
0	GPIO[0]	X1B_IRQ_EXT0#

ic_cfg0set **Address: 0x0_1180_0040**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x80000000

ic_cfg1set **Address: 0x0_1180_0048**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	1	0	0	0	1	0	0	1	0	1	1	0	1	1	1

0x280144A7

ic_cfg2set **Address: 0x0_1180_0050**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	0	1	0	0	0	1	0	0	1	0	1	1	0	1	1	1

0x280144A7

Interrupt Controller 1 Source Select Register

ic_srcset **Address: 0x0_1180_0058**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0xFFFFFFFF

Interrupt Assignment Register 1

ic_assignset **Address: 0x0_1180_0060**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
INIT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

0xFFFFFFFF

Wake up Source Selection

ic_wakeset **Address: 0x0_1180_0068**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

0x000000A0

Interrupt STAT Register 1

ic_STATset **Address: 0x0_1180_0070**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
INIT	0	1	0	0	0	1	0	0	1	0	1	0	0	1	1	1

0xA8014497

7 Appendix

7.1 ID-EEPROM Register Map

EEPROM-Content

Field	Off-set	Size (Byte)	Format	Content (hex), Example	Content (ASCII), Example	Remarks
Boot Counter	0x000	4	Binary	C8 45 00 00		Counter=17864, increased by bootloader
Manufacturing Date	0x004	6	BCD	24 12 04 20 18 15		Production Date, e.g. 24.12.2004, 18:15
Maintenance Time	0x00A	6	BCD	01 07 05 20 10 45		Last Service, e.g. 01.07.2005, 10:45
HW Platform	0x010	16	ASCII	4D 53 43 20 45 58 4D 2D 53 48 37 37 36 30 00 00	MSC EXM-SH7760	Board ID String
HW Revision	0x020	16	ASCII	34 30 2D 61 62 63 64 65 66 67 68 69 00 00 00 00	40-abcdefghi	40: V4.0 abc…: Board Revision and Variant Code
Serial Number	0x030	16	ASCII	30 33 30 30 30 39 36 30 30 31 31 2D 31 00 00 00	03000960011	10-digit series number (Also on barcode-label on the module)
User-Area	0x080	1968		User specific	User specific	

- ASCII-Fields must be terminated by 0x00.
- Binary: LSB on lowest address, ascending
- Manufacturing Date, Maintenance Time:
  - 0, when not supported
  - BCD: Day,Month,Year,Hour,Minute

Location of the ID-EEPROM

Hardware	I2C Bus	Device Adr.	Offset
EXM32 AU1250	0	0xA0	0x00

Size: 2048 Byte
Partitioning System area: 0x000 -0x07F (128 Byte)
User area: 0x080-0x7FF (11968 Byte)
Speed: 400 kHz
Protocol: 8 Bit Register-Offset